Stochastic Circuit Design for Molecular Architectonics

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Molecular structures represent an alternative to continue with the miniaturization of device sizes to the limit of molecular scales. However, there are some disadvantages, such as thermal instability and fluctuations that may lead to malfunctions in terms of systems. In such framework, based on a previous study by exploiting the Stochastic Resonance effect [1], this work proposes a scheme to implement the logic gates (SR logic gates) to overcome the problem of parameter variations for nanoscale devices working at low power consumption [2]. Although our design is based on Metal Oxide Transistors (MOS), it could be a candidate for the implementation of molecular devices where fluctuations are present.

As the response of the SR gates is dependent on stochastic processes, an unpredictable delay is present. A possible solution of this problem is found in the field of asynchronous circuits, which allows the design of delay-insensitive circuits (DI circuits) [3]. DI circuits overcomes the problem associated with unpredictable delays since their operation does not rely on a central clock for synchronization, but on handshake protocols. Moreover, asynchronous circuits allow the design of low-power circuits since its lack of clock.

In this study, we present the simulation of the basic asynchronous circuits, following a dual-rail encoding to generate a more robust design. Circuit simulations were performed using SPICE simulator for a MOS technology of 0.18 μm. The standard deviation of noise was set to 27 mV with a power supply of 0.35 V. Circuit simulations proved the constructive role of noise to recover the logic operations in the presence of variations of V_{TH}.

References

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