Artificial Life on Single-Electron Circuits

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Abstract— **A promising area of research in nanoelectronics is the development of electrical systems that imitate the dynamics of life. To proceed toward this goal, I have proposed CMOS and single-electron devices that imitates the behavior of neural networks and a reaction-diffusion system, which is a chemical complex system producing dynamic, self-organizing phenomena in the natural world [1], [2]. Constructing an electrical analog of biological systems would enables us to generate artificial bio-dynamics on a LSI chip and develop bio-inspired information processing systems. Here I briefly overview our recent results on the development of single-electron circuits that perform non-classical computation inspired by biological systems. First, a novel single-electron device for computation of a Voronoi diagram is introduced. Then I present a single-electron neural circuit for a robust synchrony detection among multiple spike inputs. This work has been extended to utilize stochastic resonance between single-electron neurons for possible robust computation on single-electron circuits. Finally, I introduce a novel semiconductor device in which electronic-analogue dendritic trees grow on multi-layer single-electron circuits, for emulating dendritic computation of neural networks on semiconductor devices. I plan for a semiconductor artificial life (brain) that might be over-ambitious – but not completely ridiculous. Our final purpose is to uncover new ideas that could help to create better processors or reveal something about the way our brain works.**

I. A single-electron reaction-diffusion device for computation of a Voronoi diagram

Computation of a Voronoi diagram (VD) is one of the typical problems in computer science, and VDs are used in graphics, statistics, geography and economics [3] and [4]. The key feature of VD construction is a partition of two- or three-dimensional space on a sphere of influences generated from a given set of objects, points, or arbitrary geometrical shapes. Here I introduce a novel single-electron device for computation of a VD. A cellular-automaton model of VD formation [5] is used to construct the device that consists of three layers of a 2-D array of single-electron oscillators.

A. Single-Electron Circuits for computation of Voronoi Diagram

For VD computation, I propose to use single-electron reaction-diffusion (SE-RD) devices. The original SE-RD device consists of arrayed single-electron oscillators and can imitate the operation of chemical RD systems [6]. Figure 1 illustrates the original SE-RD device. The main component is a single-electron oscillator that consists of a tunneling junction C_j and a high resistance R connected in series at a node and biased by a positive voltage $V_{\rm dd}$ or a negative one $-V_{\rm dd}$. It has voltage $V_{\rm node}$ of the node, and $V_{\rm node}$ shows the excitatory oscillation that is indispensable for imitating RD systems [6].

To compute a VD with RD systems, spatially localized waves that travel upon computing media at a constant speed are necessary [5], [7]; i.e., the wave-fronts must be smooth and their speed must be constant. The original SE-RD device can generate nonlinear voltage waves. However, the device was not suitable for computing a VD because the wave-fronts were not smooth, as shown in Fig. 2, and their speeds were not constant. The tunneling probability of each electron tunneling at the oscillators is the reason why the waves can not travel at a constant speed. To make the wave fronts smooth and the speed of the waves constant, new oscillators in which the probability is averaged are necessary. Therefore I have developed new oscillators with multiple-tunneling junction (MTJ) as shown in Fig. 3. The MTJ oscillator consists of a multiple-tunneling junction $C_{\rm m}$ that has n tunneling junctions and a high resistance R connected in series at the node and biased by $V_{\rm dd}$. It has a voltage $V_{\rm node}$ that shows the excitatory oscillation like the original oscillator does. There are many tunneling junctions in the oscillator, so the tunneling probability is averaged. As a result, $V_{\rm node}$ changes smoothly as shown in Fig. 3 (b). The improved SE-RD device has such oscillators.

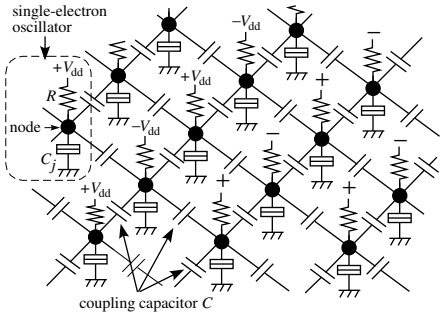

Fig. 1. Circuit configuration of single-electron reaction-diffusion device [6].

Fig. 2. Spatially-localized voltage wave that is generated by the original SERD device (simulated). The device has 100 × 100 oscillators. Simulated with parameters: tunneling junction capacitance $C_{\rm j}$ = 1 aF, tunneling junction conductance = 1 μS, high resistance R = 137.5 MΩ, coupling capacitance C = 1 aF, bias voltage $V_{\rm dd}$ = 16.5 mV, and zero temperature. In this figure, high voltage is bright and low voltage is dark [6].

Adjacent oscillators have to be coupled with a capacitor for the voltage waves to travel on the improved device. Figure 4 shows simulation results of a one-dimensional chain of improved oscillators. The oscillators that in the figure are denoted by A1, A2,..., with their nodes represented by closed circles are connected to their adjacent oscillators through intermediary oscillators that are biased by a negative voltage $-V_{\rm dd}$ (these are denoted by B1, B2, ..., with their nodes represented by open circles) and coupling capacitors C (Fig. 4 (a)). When electron tunneling occurs in an oscillator in this structure, the node voltage of the oscillator decreases gently, and this induces electron tunneling in an adjacent intermediary oscillator. The induced tunneling changes the node voltage of the intermediary oscilla-

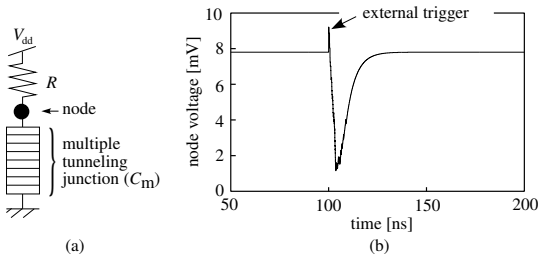

Fig. 3. Single-electron oscillator with multiple-tunneling junction. (a) circuit configuration and (b) its operation (simulated). Simulated with parameters: tunneling junction capacitance $C_m = 10$ aF (500 aF/50 junctions), tunneling junction conductance = 5 μS, high resistance $R = 20$ GΩ, bias voltage $V_{dd} = 7.8$ mV, and zero temperature.

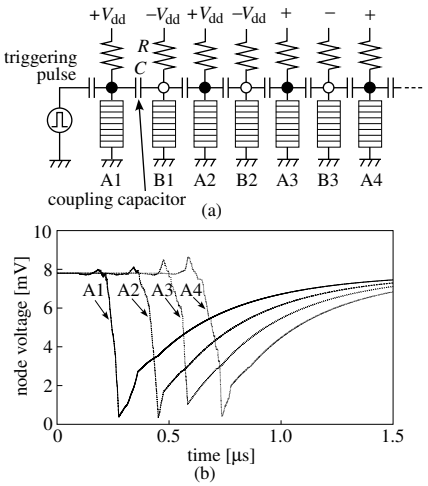

Fig. 4. One-dimensional chain of improved oscillators. (a) circuit configuration and (b) its operation (simulated). Simulated with parameters: tunneling junction capacitance $C_m = 10$ aF (500 aF/50 junctions), tunneling junction conductance = 5 μS, high resistance $R = 20$ GΩ, coupling capacitance $C = 2.2$ aF, bias voltage $V_{dd} = 7.8$ mV, and zero temperature.

tor from low to high, and this induces electron tunneling in an adjacent oscillator. As a result, changes in node voltage that are caused by the electron tunneling are transmitted from one oscillator to another along the oscillator chain (Fig. 4 (b)). Note that the voltage waves travel at almost constant speed. This is because the tunneling probability is averaged over all oscillators.

An improved SE-RD device can be constructed by connecting oscillators into a network by means of intermediary oscillators and coupling capacitors as shown in Fig. 5. Each oscillator is connected to its four adjacent oscillators by means of four intermediary oscillators and coupling capacitors. Nonlinear voltage waves travel on the improved device at a constant speed as shown in Fig. 6. One can compute the VD by using information on collision points of the nonlinear waves for which I use CA model [5], [7] for finding collision points. In the CA model, a cell that connects eight adjacent cells changes its state according to the states of the adjacent cells. The cell state transition rule is as follows:

$$x^{t+1} = \begin{cases} \beta, & \text{if } x^t = \bullet \text{ and } 1 \le \sigma(x)^t \le 4 \\ \alpha, & \text{if } x^t = \beta \text{ and } 1 \le \sigma(x)^t \le 4 \\ x^t, & \text{otherwise} \end{cases}$$

where x is the state of the middle cell, t is the time step, $\bullet$ is a resting cell, α is colored precipitate, β is reagent and $\sigma(x)^t$ is

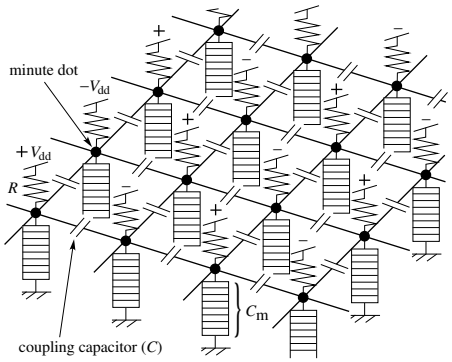

Fig. 5. Improved two-dimensional RD device consisting of network of improved single-electron oscillators. Each oscillator is connected with four neighboring oscillators by means of four intermediary oscillators and coupling capacitors.

Fig. 6. Traveling nonlinear wave that is generated by the improved SE-RD device (simulated). 50 × 50 oscillators are placed in the device. This simulation used the same parameters as in Fig. 4 (b). In this figure, high voltage is bright and low voltage is dark.

the number of β cells in the eight adjacent cells. In this model, the collision points are memorized as the precipitate of reagents.

To apply this rule to our device, I use single-electron threshold detectors, specifically the single-electron boxes (SEB) that I have proposed as logic gate devices [8], [9]. The SEB consists of a single-electron trap (two identical tunneling junctions C_j, connected in series, a capacitor C_L and a bias voltage V_{dd}) as shown in Fig. 7 (a). This circuit has a hysteretic sawtooth function for V_{dd} as shown in Fig. 7 (b). I made use of this characteristic for threshold operation.

Let us consider the threshold operation for computing a VD based on the CA model, and assume the threshold value that is the number of β cells in the eight adjacent cells to be 4.5; i.e., no electron tunneling occurs in the SEB when the node voltages of four or fewer adjacent oscillators are changed by electron tunnelings in the oscillators. On the other hand, electron tunneling occurs in the SEB when the node voltages of five or more adjacent oscillators are changed. In addition, one can find the collision points by comparing the state of the center oscillator with the state of the SEB threshold detector. To compare the states, I used the SEB with the threshold set to 1.5; i.e., no electron tunneling occurs in the SEB when electron tunnelings occur in both the above SEB and the center oscillator.

Figure 8 shows an improved device with three layers for computing a VD. The top layer ((a) in Fig. 8) is the improved SE-RD device shown in Fig. 5. The middle layer ((b) in Fig. 8) is the first logic layer of SEB threshold detectors. Here, the SEB that is biased by the negative voltage $-V_{b1}$ ((e) in Fig. 8) are placed directly under the oscillators biased by $+V_{dd}$ (oscillator 9 in Fig. 8) and connects to the eight adjacent oscillators of the top layer (oscillators 1–8 in Fig. 8 (d)); i.e., the SEB accepts eight signals from the eight oscillators as inputs. The bottom layer ((c) in Fig. 8) is the second logic layer. The SEB that is

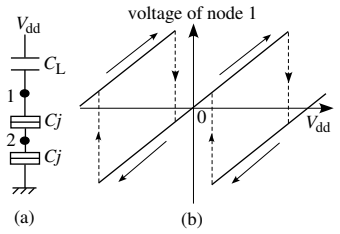

Fig. 7. Single-electron box. (a) Circuit configuration and (b) its operation [8], [9].

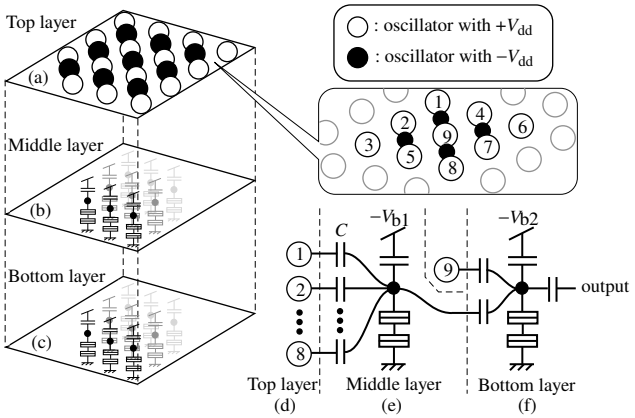

Fig. 8. Improved device that has three layers for computing a VD. The top layer is the device shown in Fig. 5. The middle layer is the first logic layer with SEB threshold detectors. The bottom layer is the second logic layer and it produces the VD.

biased by the negative voltage $-V_{b2}$ ((f) in Fig. 8) connects to the oscillator 9 and the SEB in the second layer ((e) in Fig. 8); i.e., the second SEB accepts two signals from the oscillator 9 and the SEB in the second layer as inputs. The bottom layer produces the output; i.e., its output is used to draws the VD.

B. Simulation Results

Figures 9, 10 and 11 show the simulation results, while Fig. 9 shows the density of node voltages on the top layer. A bright color means the node voltage is high. A dark color means the node voltage is low. Figures 10 and 11 show the voltages on the middle layer and on the bottom layer. In Fig. 10, 'A' indicates the wave-front in the top layer, 'B' indicates the wave-front in the middle layer, and 'C' indicates collision points. In this simulation, I triggered three oscillators of the top layer as planar points for a VD. Nonlinear voltage waves traveled at a constant speed and gave the data to the middle and bottom layers. In the middle layer, the SEBs changed their node voltage when five or more oscillators of the upper eight oscillators changed their node voltage. Wave-fronts in the top layer had four or fewer oscillators that changed their voltages. As a result, traveling nonlinear waves in this layer (B in Fig. 10) followed the waves in the top layer (A). When wave 'A' collided with other waves in the top layer, the collision points had five or more oscillators that changed their voltages. Therefore, wave 'B' in this layer overtook 'A' and collided with other waves just like spanning a valley with a bridge (C). In the bottom layer, the SEBs changed their node voltages when both the voltage of the oscillators in the top layer and the SEBs in the middle layer are low. Namely, traveling waves that did not collide were memorized by the bottom layer as a high voltage. When the nonlinear waves of the top layer collided with each other, the voltages of the collision

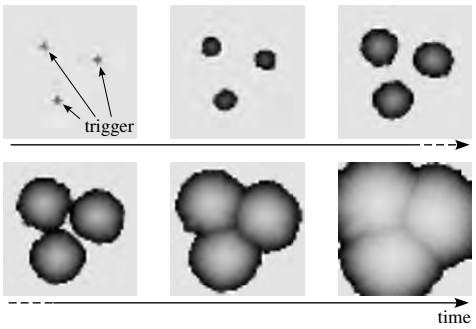

Fig. 9. Expanding circular pattern in the top layer of the device. Snapshots for six time steps. The simulation used the same parameters as in Fig. 4 (b) for the simulation.

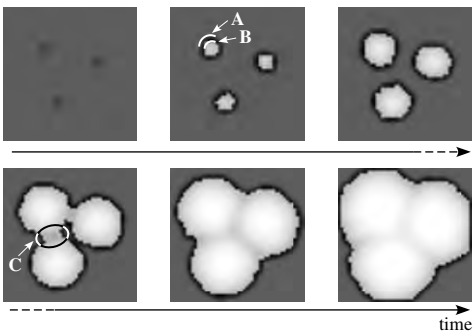

Fig. 10. Expanding circular pattern in the middle layer of the device. Snapshots for six time steps. Parameters: tunneling junction capacitance $C_j = 20$ aF, tunneling junction conductance $= 5$ μS, bias capacitance $C_L = 10$ aF, coupling capacitance $C = 2.2$ aF, bias voltage $V_{b1} = 26.5$ mV, and zero temperature.

points in the top were low and the node voltages of the SEBs in the middle were high. As a result, the node voltages of the SEB in the bottom were kept low. Therefore, the bottom layer memorized the result of computing the VD.

II. Single-Electron Synaptic Depression

Synaptic depression, network dynamics, and their applications have recently attracted the attention of many modelers who mainly focused on the dynamic implications of neural systems. Abbott et al., for example, reported a striking feature of synaptic transmission between neurons [10] where postsynaptic firing rates for input spike trains are limited at some value because of short-term synaptic depression. Furthermore, interesting applications of various neural networks with depressing synapses have also been proposed [11], [12], [13], and various hardware synapses on neuromorphic CMOS devices have been fabricated [14], [15]. Such neuromorphic devices can be expected to be high-functioning information processing devices in the future. This section describes our design of a single-electron depressing synapse (SEDS) on a single-layer nanodot array, showing that device implementation of the SEDSs on such a nanodot array is much easier than the implementation of depressing synapses on CMOS VLSIs.

A. Single-electron depressing synapse circuit

In designing a SEDS, I use a pair of single-electron oscillators (Fig. 13) that I proposed for use in designing an excitable media [6] and a spiking neuron circuit on a single-layer nanodot array [16]. The oscillator has excitatory, refractory, and

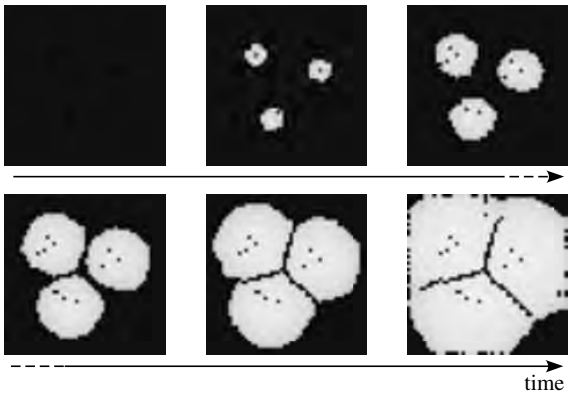

Fig. 11. Expanding circular pattern in the bottom layer of the device. Snapshots for six time steps. Traveling nonlinear waves in this layer construct a VD. Parameters are the same as in Fig. 10 without bias voltage $V_{b2} = 18.5$ mV.

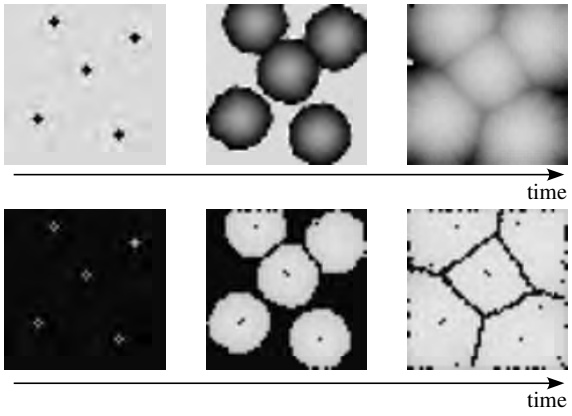

Fig. 12. Simulation results of computing a VD with five planar points by using proposed device. Upper three snapshots show the voltage density of the top layer, and the bottom three snapshots show the voltage density of the bottom layer.

resting periods. Here I propose the use of refractory properties of spiking neurons, where the neuron cannot fire continuously for high-frequency input spike trains, as depressing characteristics of the SEDS; i.e., I regard an array of spiking neurons as a depressing synapse because input spike trains are depressed by each neuron operating in its refractory period. Therefore, one can use an array of single-electron oscillators to construct the SEDS. It should be noted that the term of the refractory period increases as values of gNa and gK increase [6].

There is a neuromorphic relationship between the proposed SEDS and electronic Hodgkin-Huxley (H-H) models: i) a tunneling junction (C_j) corresponds to a membrane capacitance and voltage-controlled gates in H-H models, ii) nonlinear chemical reactions between Na+ and K+ can be mediated by a coupling capacitance (C) because of the neuron's dielectric inside the soma.

B. Results

The depressing properties of a single SEDS were examined by numerical simulations. I used typical parameter values for the single-electron circuit [6], except for gNa ($= g$K) $= 5$ μS, 2.5 μS and 1 μS. Figure 14 shows synaptic conductivities ($\sim$ the number of postsynaptic spikes) for interspike intervals (ISI) of input spike trains. As the ISI increases, the conductivity

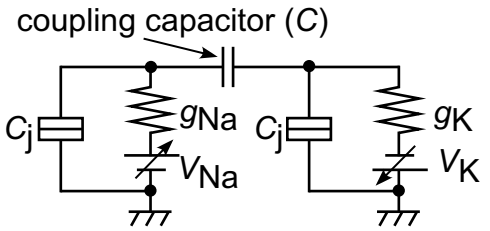

Fig. 13. Pair of single-electron oscillators corresponding to neuronal membrane.

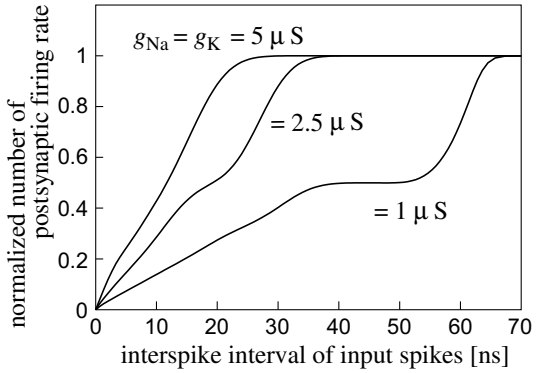

Fig. 14. Synaptic conductivities ($\sim$ the number of postsynaptic spikes) for interspike intervals (ISI) of input spike trains.

increases because each SEDS can easily be recovered from its depressed (refractory) period as the ISI increases. Because the depressed period increases as gNa and gK increase, the SEDS's conductivity for increasing ISIs decreases significantly.

III. Stochastic Resonance among Single-Electron Neurons on Schottky Wrap-Gate Devices

Neuromorphic computing based on single-electron circuit technology has become widely noticed because of the recent claim about its massively increased computa- tional efficiency and its increasing relevance between computer technology and nanotechnology. Its impact will be strongly felt when single-electron circuits based on a fault- and noise-tolerant neural structure are able to operate in a room-temperature environment. To fabricate such robust single-electron devices, I investigated stochastic resonance (cf. [17]) in an ensemble of single-electron boxes (SEB) [18]. I employed a single- electron transistor (SET) on a schottky wrap-gate (WPG) device [19], instead of a SEB, as a neuron, and examine statistical results of the network by numerical simulation.

The reason why I employ WPG-SETs instead of SEBs is that SETs have a switching characteristic as CMOS transistors do. A general SET consists of a capacitor (C) for an input terminal and two tunneling junctions (C_js), as shown in Fig. 15. A SET has three terminals, and one can connect controllable voltage sources to the terminals. Now let us connect terminals with bias V_d, input V_g and ground, respectively, and controll the switching characteristic by controlling the voltage sources. When the SET is in operation, an electron can tunnel through two C_js (between ground and a node, or between a node and V_d) in a low-temperature environment because electron tunneling is governed by the physical phenomenon called the Coulomb blockade effect. In addition, one can easily observe the operations of practical SET devices. However, we must also be careful

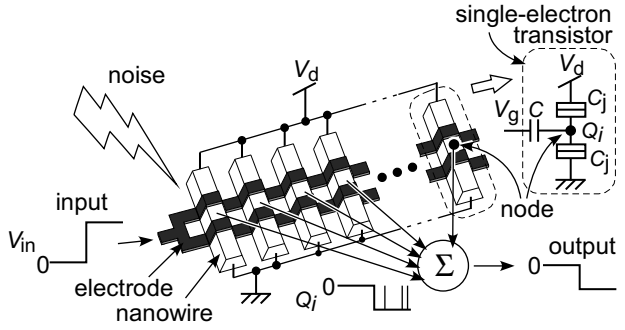

Fig. 15. Schematic image of SET array.

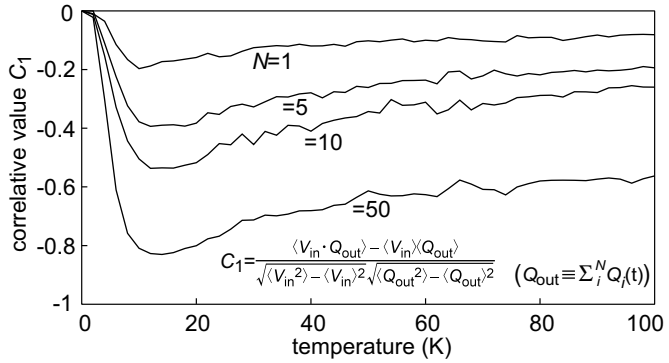

Fig. 16. Stochastic resonance in ensemble of single-electron transistors.

when we use single-electron circuits in a high-temperature environment. The reason is that electrons randomly tunnel through C_js because the Coulomb blockade effect is disturbed by thermal fluctuations.

Let us consider an SR among N SETs in a network, as shown in Fig. 15. When SETs are not connected with each other, electron tunneling in each SET's junction occurs independently. As in [17], I applied a common input to all the SETs and calculated the sum of outputs of the SETs. For simplicity, I applied a common input voltage V_{in} to all the SETs as V_g, and did not consider practical circuits that calculate the sum of the changes in each node's electric charge Q_i. The i-th SET's charge (Q_i) was increased with the input voltage, while the magnitude of the input was set to a very low value so that no electron would tunnel through C_js. Under this condition, increasing the magnitude of thermal noise (temperature) enables electrons to tunnel through each C_j.

Figure 16 shows simulation results of an ensemble of SETs for $N = 1$, 5, 10 and 50. The temperature was increased from 0 K to 100 K and correlation values (C_1) between the input voltages and the summed output were calculated. The results showed characteristic signatures of SR-type behavior: a rapid rise to a peak, and then a decrease at high temperatures. One could observe that the magnitude of $|C_1|$ increased as N increased, as expected. The resonant temperatures were approximately 10 K for all the values of N. In addition, C_1 took a large value -0.6 at 100 K when $N = 50$, and increased as N increased. According to [17], the correlation value should become almost 1.0 when $N = 1000$. The results indicate that when one employs such an SR network in single-electron circuits, it certainly acts as a transmission line that can cancel noises on the line, as well as, cancel the devices' intrinsic noises.

IV. Single-electron circuits performing dendritic pattern formation with nature-inspired cellular automata

Ordered complex patterns can easily be observed everywhere in the natural world. Among these, bifurcated and branched patterns formed in open systems often serve as a basis for advanced functional structures. Indeed, these structures are essential for performing particular computational tasks in nature, e.g., structures of a neuron's dendritic tree are responsible for various intelligent computing tasks. Recent advances in neuroscience have revealed that fundamental roles of these dendritic trees include not only the transmission of neuronal signals but also functional computation utilizing multiple properties of membranes and spines (early works can be found in [20] and [21]). To incorporate the functions performed by dendritic trees into neuromorphic hardware, I develop a single-electron circuit that selforganizes spatial dendritic patterns on a multilayer nanodot array. As the first step, I propose a cellular automaton (CA) model based on a behavioral model of bacteria colonies [22].

It is difficult to implement a huge amount of physical wiring, i.e., axons and dendrites, on a 2-D semiconductor chip because the wiring is fabricated by stacking several layers of only wiring. Here I use single-electron circuits, which are believed to have potential for next-generation VLSIs, to increase the wiring density. I also actively incorporate quantum effects and sensitivity to thermal noise into the design of compact unit circuits for the proposed CA.

A. Model of cellular automata for generating dendritic patterns

One of features of neurons is the complexity of their forms, such as tree-like, branching dendritic form. The details of dendritic pattern formation in neural systems have been mainly studied from the viewpoint of molecular biology, rather than that of general physics. This kind of branching pattern is also observed in many other systems, including trees, crystal growth, protoplasmic streaming tubes of slime molds, bacterial colonies, and so on. Due to generality of these kinds of patterns several models have been proposed to describe complex branching patterns [23], [24], [25]. One of the best-known simple models is the diffusion limited aggregation (DLA) model [23]. Another well-known type of model is the reaction-diffusion (RD) model for the pattern formation of bacterial colonies, which exhibit more diverse patterns than the DLA model [25]. Two methods are used to describe RD systems; one is based on partial differential equations (PDE) [26] and the other on discretized CA [27]. Space, time, and state variables are generally discrete in the CA model, whereas they are continuous in the PDE representation of the RD system. Here I use CA representation of RD dynamics based on bacterial colony pattern formation to represent dendritic patterns because of the variety of patterns available and its expansibility for device applications.

The skeleton of the RD pattern formation model of a bacterial colony consists of movement/schism of bacteria, diffusion of nutrients, and consumption of nutrients by the bacteria. In the model, the dynamics are described as "reaction", the relationship of the bacteria and the nutrient, and "diffusion", which averages the bacteria or nutrient in the neighborhood. In CA models, the targeted space is divided into discrete areas of named cells. The time evolution of the state of each cell is decided by simple inner- and inter-cell rules, and a dynamic pattern or whole structure is generated from these local interaction rules. The algorithm of our CA model is as follows. Three variables are used to describe the state of the system in each

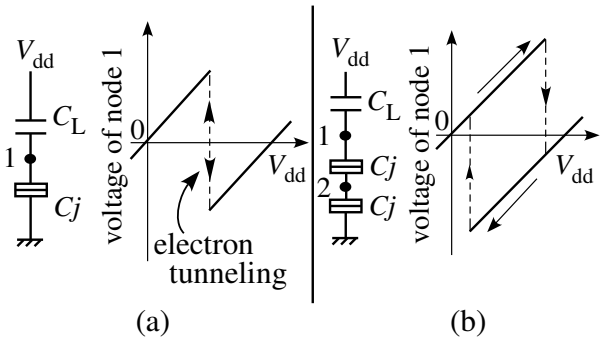

Fig. 17. Single-electron devices. (a) single-electron box, and (b) single-electron memory circuit.

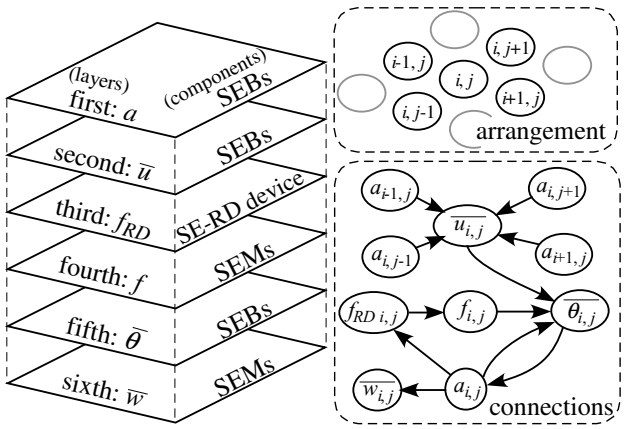

Fig. 18. Single-electron device for generation of dendritic patterns.

cell; active bacteria (activator) a, inactive bacteria (inactivator, a trace of activator) w, and nutrient (substrate) f. The variables a and w take the digit value {0,1}, and f takes a digit or multi-value. When there are both a sufficient number of activators in the cell's neighborhood and sufficient substrate in the cell, the state of the activators becomes 1 ($a : 0 \rightarrow 1$), and substrate f is depleted in the next step. After ($a \rightarrow 1$), when the substrate in the cell itself is less than the threshold value as a result of depletion, the activator can no longer sustain an active state, the state of the activators becomes 0 ($a \rightarrow 0$), and the state of the inactivator becomes 1 ($w \rightarrow 1$). The substrate diffuses constantly with fluctuation. When there is insufficient substrate, the activators try to take up the limited substrate. As a result, the cluster of activators divides into several clusters, and a branching pattern appears as the cluster of cells, where inactivator $w = 1$.

B. Single-electron device for generating dendritic patterns

To imitate the diffusion of the consumed substance with fluctuation in the model, I used a single-electron reaction-diffusion (SE-RD) device [6], single-electron boxes (SEBs), and single-electron memory (SEM) circuits [9] to implement the CA rules. A typical single-electron circuit consists of tunneling junctions, resistances, and capacitors. A tunneling junction that is similar to a capacitor is main component of a single-electron circuit. In a junction, a quantum effect occurs. A point of difference between tunneling junctions and normal capacitors is that the two conductors of the junction face each other very closely. The junction has a threshold voltage value for the generation of a quantum effect that is electron tunneling. A single-electron passes through the junction when the junction potential is over the threshold voltage, and the potential of the junction changes suddenly. The tunneling event has a probability of occurring, given by

$$P(E) \sim \frac{1}{1 - \exp[-\Delta E/(k_B T)]} \tag{1}$$

where P is the tunneling probability, E is the charging energy, k_B is the Boltzmann constant, and T is the temperature. The equation has a temperature factor. Therefore, the tunneling probability changes with the temperature. I would like to utilize this physical phenomenon to implement fluctuation in the diffusional operation of the CA model. The circuit configuration and example operations of a SE-RD device have already been shown in Figs. 1 and 2, respectively.

I used SEBs to change the input signals to binary signals. The left of Fig. 17(a) shows the circuit configuration of an SEB. It consists of a tunneling junction, bias capacitor, and bias voltage source. The right of Fig. 17(a) shows a sample operation. The SEB shows a positive voltage (logical 1) when no electron tunneling occurs, and a negative one (logical 0) when electron tunneling occurs. I also used SEMs as memory devices because they have a hysteretic function as a function of the input voltage. The left of Fig. 17(b) shows the circuit configuration of an SEM. It consists of two tunneling junctions, a bias capacitor, and a bias voltage source, in series. The right of Fig. 17(b) shows a sample operation [9]. The SEBs and SEMs play the role of active and inactive bacteria, respectively.

I designed a new single-electron device based on the CA model, the SE-RD device, the SEBs, and the SEMs. The device consists of six layers (Fig. 18). I added two factors "$u_{i,j}$" and "$\theta_{i,j}$" to the device as supplementary functions. The first layer consists of arrayed SEBs that implements the "$a_{i,j}$" of the model. The second also consists of arrayed SEBs that implement the added factor "$u_{i,j}$". The third is the SE-RD device, and the fourth consists of arrayed SEMs. The third layer implements "$f_{i,j}$" in collaboration with the fourth layer. In this device, f takes a digit value. The fifth layer consists of arrayed SEBs that implement the added factor "$\theta_{i,j}$", and the sixth consists of arrayed SEMs that implement the "$w_{i,j}$" of the model. The unit circuits of each layer are assumed to be cells of the CA. The operations of each factor are represented by the following equations:

$$a_{i,j} = \begin{cases} 1 & (\text{if } \theta_{i,j} = 1) \\ 0 & (\text{otherwise}) \end{cases} \tag{2}$$

$$u_{i,j} = \begin{cases} 1 & (\text{if } a_{i-1,j} + a_{i+1,j} + a_{i,j-1} + a_{i,j+1} = 1) \\ 0 & (\text{otherwise}) \end{cases} \tag{3}$$

$$f_{RD\ i,j} = \begin{cases} \text{TN} & (\text{if } a_{i,j} = 1 \text{ or neighbor } f_{RD} = \text{TN}) \\ \text{NT} & (\text{otherwise}) \end{cases} \tag{4}$$

$$f_{i,j} = \begin{cases} 0 & (\text{if } f_{RD\ i,j} = \text{NT or } f_{i,j} = 0) \\ 1 & (\text{otherwise}) \end{cases} \tag{5}$$

$$\theta_{i,j} = \begin{cases} 1 & (\text{if } \overline{a_{i,j}} \cdot u_{i,j} \cdot f_{i,j} = 1) \\ 0 & (\text{otherwise}) \end{cases} \tag{6}$$

$$w_{i,j} = \begin{cases} 1 & (\text{if } a_{i,j} + w_{i,j} = 1) \\ 0 & (\text{otherwise}) \end{cases}, \tag{7}$$

where 'TN' and 'NT' represent 'tunneling' and 'no tunneling', respectively.

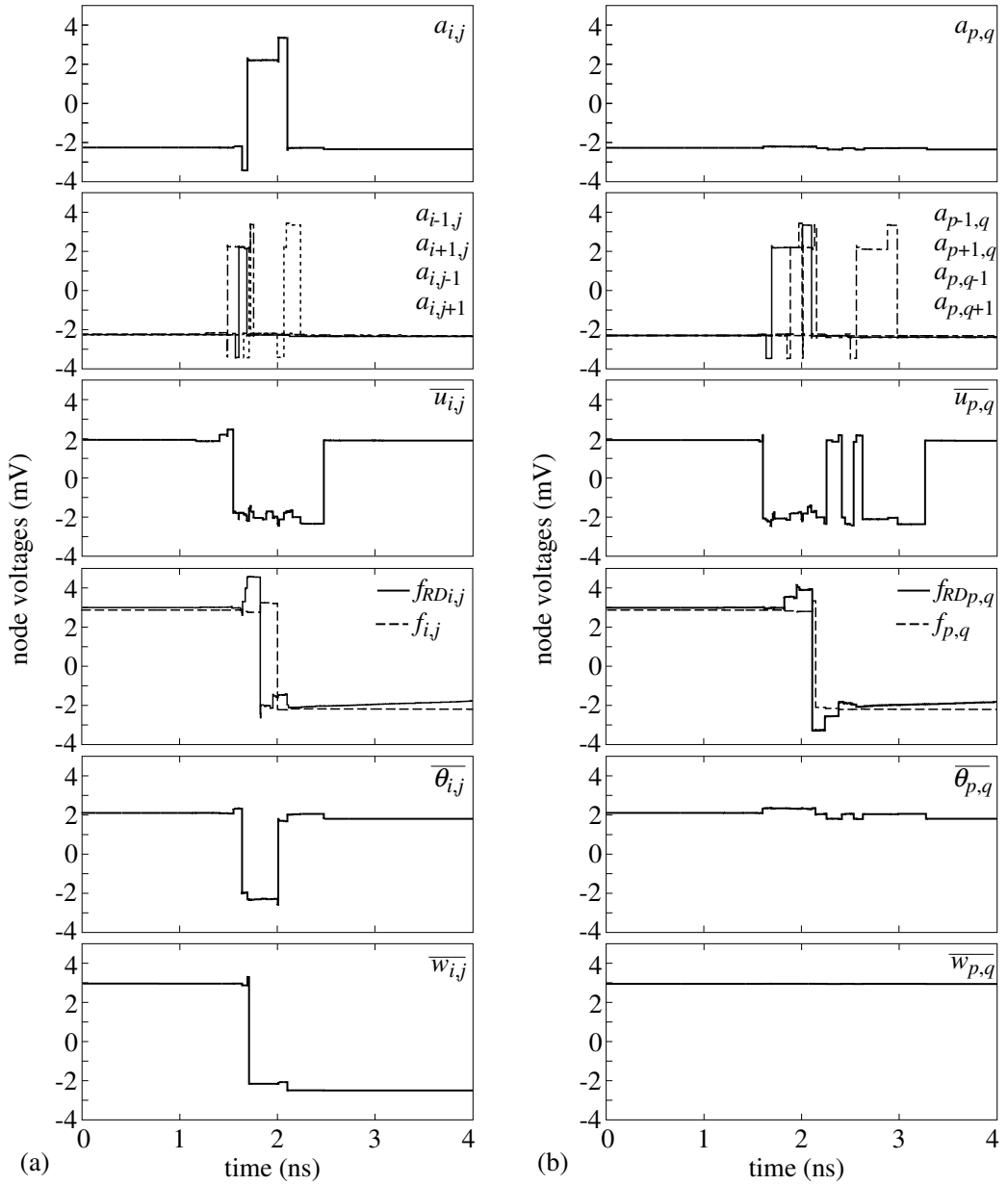

Fig. 19. Simulation results. (a) correct operations, (b) failed operations.

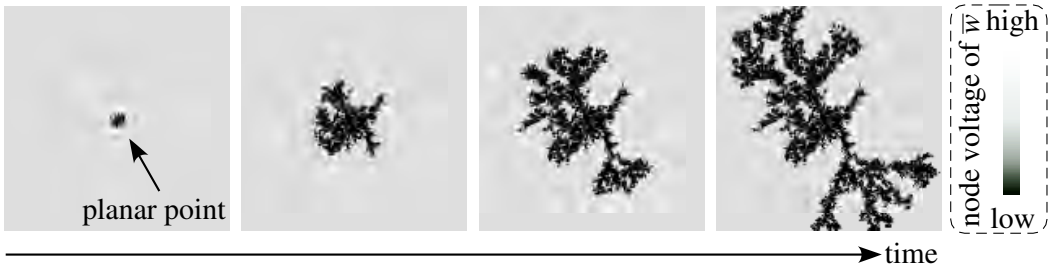

Fig. 20. Result of two-dimensional simulation of sixth layer.

C. Results

In the simulation, the device had 200 × 200 elements in each layer. Figure 19 shows sample operations of the elements in each layer. In Fig. 19 (a), $a_{i,j}$ maintained a logical 0 state (negative voltage) until $\theta_{i,j}$ changed its 0 state to 1 (positive voltage). $u_{i,j}$ kept 0 state until neighbor a changed its 0 state to 1. $f_{i,j}$ ($f_{RD\ i,j}$) maintained 1 state until $a_{i,j}$ changed its 0 state to 1 or electron tunneling occurred in the neighboring f_{RD} and kept 0 state after it changed its state from 1 to 0. $w_{i,j}$ kept 1 state until $a_{i,j}$ changed its 0 state to 1 and kept 0 state after it changed

its state from 1 to 0. Thus, the device implemented the CA model. However, operating errors sometimes occurred because of the tunneling probability in the device. Figure 19 (b) shows sample operations. In the figure, p and q represented different points from i and j. Neighbors a, $u_{p,q}$, and $f_{p,q}$ operated well as did a, u, f in Fig. 19 (a). $\theta_{p,q}$, however, showed a failed operation because of the tunneling probability. As a result, $a_{p,q}$ and $w_{p,q}$ could not change their state. This failed operation works as the diffusion of the consumed nutrient with fluctuation in the model. Figure 20 shows the results of a two-dimensional simulation. In the simulation, a spatiotemporal pattern was formed on the sixth (w) layer. The pattern grew from a planar point, but some parts of the growing points stopped because of both the correct and failed operations in each layer. As a result, a dendritic pattern appeared. This dendritic pattern will change with every simulation because of the tunneling probability.

V. SUMMARY

First, I introduced a single-electron reaction-diffusion devices for computing a Voronoi diagram. The novel SE-RD device consists of three layers. The top layer is an improved SE-RD device in which nonlinear voltage waves are generated and travel, and the middle and bottom layer are threshold detectors. The operations of the middle and bottom layer are based on the CA model [5], [7]. The bottom layer outputs the results of computing a VD by using data from the top and middle layers.

Second, a single-electron depressing synapse and its characteristics was introduced for considering possible applications on noise-tolerant synchrony detection. Previous works on CMOS VLSI showed that the network had great noise-tolerant ability for static noise embedded as device (threshold) mismatches of MOSFETs [28]. I expanded this notion to dynamic ones that are usually a common problem in the area of single-electron circuits. The results showed that the performance is greatly increased by increasing the temperature until T $\leq$ 0.5 K [29]. However, all of the parameter sets are not optimized. The performance is apparently sensitive to the time constant of a single-electron oscillator and interspike intervals of input burst spikes. Our next goal is an appropriate theory for the emergence of the noise tolerance and optimization of these parameters to explore the possible development of faultand noise-tolerant single electron computing devices.

Third, stochastic resonance (SR) in an ensemble of single-electron neuromorphic devices was introduced. Recently I have proposed a single-electron competitive neural network based on SR in an ensemble of single-electron boxes that can operate at room temperature [18]. Using realistic physical parameters, I confirmed the SR behavior of single-electron boxes. The resonant temperature was 20 K, independent of the number of boxes (N). Using numerical simulations, we demonstrated that the winners and losers of the SR based network ($N = 50$) can be discriminated even at room temperature.

Finally, I introduced novel single-electron circuits for forming dendritic patterns. To construct the proposed device, I designed a six-layer single-electron circuit with nature-inspired cellular automata. The utilized cellular automaton had three factors. In the device, the top, second, and fifth layers consist of arrayed single-electron boxes, the fourth and sixth layers consist of arrayed single-electron memory circuits, and the third layer is a single-electron reaction-diffusion device. Each layer described each factor of the CA rule with randomness. As a result, the device formed dendritic patterns in the sixth layer. These patterns will change with variations in the circuit parameters or temperature environment.

References

[1] Adamatzky, A., De Lacy Costello, B., and Asai, T.: *Reaction Diffusion Computers*. Elsevier, UK (2005).

[2] Asai, T.: A neuromorphic CMOS family and its application. Brain-Inspired IT I, International Congress Series, Vol. 1269, pp. 173-176, Elsevier, Netherlands (2004).

[3] Klein, R.: *Concrete and Abstract Voronoi Diagrams*. Springer-Verlag, Berlin (1990).

[4] Okabe, A., Boots, B., Sugihara, K., and Chiu S. N.: *Spatial Tesselations: Concepts and Applications of Voronoi diagrams*. John Wiley and Sons, Chichester (2000).

[5] Adamatzky, A.: Reaction–diffusion algorithm for constructing discrete generalized Voronoi diagram. Neural Netw. World. **6** (1994) 635–643.

[6] Oya, T., Asai, T., Fukui, T., and Amemiya, Y.: Reaction-diffusion systems consisting of single-electron circuits. Int. J.Unconventional Computing. **1** (2005) 177–194.

[7] Adamatzky, A.: Voronoi–like partition of lattice in cellular automata. Mathl. Comput. Modelling. **23** (1996) 51–66.

[8] Oya, T., Asai, T., and Amemiya, Y.: Single-electrron logic device with simple structure. Elec. Lett. **39** (2003) 965–967.

[9] Oya, T., Asai, T., Fukui, T., and Amemiya, Y.: A majority-logic device using an irreversible single-electron box. IEEE Trans. Nanotech. **2** (2003) 15–22.

[10] L. F. Abbott, J. A. Varela, K. Sen, and S. B. Nelson, *Science*, Vol. 275, pp. 220-224, 1997.

[11] G. Bugmann, *BioSystems*, Vol. 67, pp.17-25, 2002.

[12] W. Senn, I. Segev, and M. Tsodyks, *Neural Computation*, Vol. 10, pp. 815-819, 1998.

[13] H. Cateau and T. Fukai, *Neural Networks*, Vol. 14, pp. 675-685, 2001.

[14] C. Rasche and R. H. R. Hahnloser, *Biological Cybernetics*, Vol. 84, pp. 57-62, 2001.

[15] S.-C. Liu, *EURASIP J. Appl. Signal Processing*, Vol. 7, pp. 620-628, 2003.

[16] T. Oya, T. Asai, R. Kagaya, T. Hirose, and Y. Amemiya, "Neuromorphic single-electron circuit and its application to temporal-domain neural competition," *Proc. 2004 Int. Symp. Nonlinear Theory and its Application (NOLTA)*, pp. 235-239, 2004.

[17] Collins J. J., Chow C. C., and Imhoff T. T., "Stochsatic Resonance without tuning," *Nature*, vol. 376, pp. 236-238 (1995).

[18] R. Kagaya, T. Oya, T. Asai, and Y. Amemiya, "Stochastic resonance in an ensemble of single-electron neuromorphic devices and its application to competitive neural networks," *Proc. 2005 Int. Symp. Nonlinear Theory and its Application (NOLTA)*, pp. 329-332, 2005.

[19] S. Kasai, K. Jinushi, H. Tomozawa and H. Hasegawa, "Fabrication and Characterization of GaAs Single Electron Devices Having Single and Multiple Dots Based on Schottky In-Plane-Gate and Wrap-Gate Control of Two-Dimensional Electron Gas," *Jpn. J. Appl. Phys.*, Vol. 36, pp. 1678-1685, 1997.

[20] Mel, B. W. (1992). NMDA-Based pattern discrimination in a modeled cortical neuron. *Neural Comput.* **4**: 502–516.

[21] Blackwell, K.T., Vogl, T.P., and Alkon, D.L. (1998). Pattern matching in a model of dendritic spines. *Network: Comput. Neural Syst.* **9**: 107–121.

[22] Motoike, N. I. (2004). Generic modeling of dendritic pattern formation with cellular automaton and the property of excitation signal propagation. *Proc. the 5th Int. Conf. Biological Physics*: 133.

[23] Witten, T. A. and Sander, L. M. (1981). Diffusion-Limited Aggregation, a Kinetic Critical Phenomenon. *Phys. Rev. Lett.* **47**: 1400–1403.

[24] Carmeliet, P. and Tessier-Lavigne, M. (2005). Common mechanisms of nerve and blood vessel wiring. *Nature (London)* **436**: 193–200.

[25] See, e.g., Mimura, M., Sakaguchi, H., and Matsushita, M. (2000). Reaction–diffusion modelling of bacterial colony patterns. *Physica A* **282**: 283–303.

[26] Turing, A. M. (1952). The chemical basis of morphogenesis. *Phil. Trans. R. Soc. Lond.* **B 237**: 37–72.

[27] See, e.g., Gerhardt, M., Schuster, H., and Tyson, J. J. (1990). Cellular automaton model of excitable media II: Curvature, dispersion, rotating waves and meandering waves. *Physica D* **46**: 392–415.

[28] T. Asai, Y. Kanazawa, T. Hirose, and Y. Amemiya, "A MOS circuit for depressing synapse and its application to contrast-invariant pattern classification and synchrony detection," in *Proc. 2004 Int. Joint Conf. Neural Networks*, W107, 2004.

[29] T. Oya, T. Asai, R. Kagaya, and Y. Amemiya, "Noise performance of single-electron depressing synapses for neuronal synchrony detection," in *Proc. 2005 Int. Joint Conf. Neural Networks*, pp. 2849-2854, 2005.

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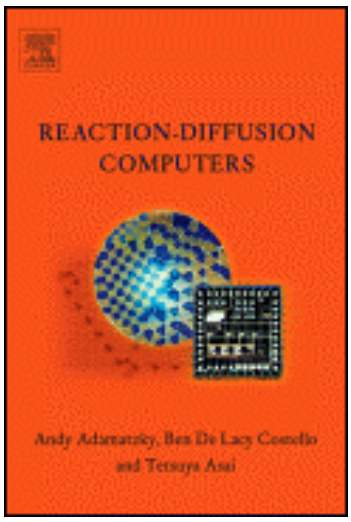

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