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ゆらぎ利用しきい論理素子による非同期式論理回路の設計

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あらまし　電子回路の低電力化のために電源電圧を下げる, または精度の低いナノ素子などを使って大規模回路を構成する場合、素子のバラツキが問題となる。本報告では、この問題を「確率共鳴」と呼ばれる非線形現象により緩和する一手法を提案する。二重井戸ポテンシャル系をラッチ型回路により構成し、そこで確率共鳴を起こすことで、素子バラツキと素子の出力の揺らぎを同時に緩和する。具体的には、しきい論理を用いて基本論理ゲートを構築し、しきい素子としてラッチを用いる。この論理ゲートが動作しなくなるような素子バラツキがある場合でも、このラッチに最適強度の雑音を与えると、確率的に正しい状態へ遷移するようになる。また、ラッチのヒステリシス特性により、正しい状態への遷移後は、その状態が雑音の擾乱を受けずに保持される。確率共鳴によりこのような現象が起こるため、この回路を「確率共鳴ゲート」と呼ぶ。しかし、確率共鳴ゲートの状態遷移のタイミング（出力が確定するまでの時間, 遅延時間）は予測できないため、この確率共鳴ゲートは同期式回路には使えない。そのため、論理素子の遅延時間に無頓着な非同期回路の一種である「ハフマン回路」に確率共鳴ゲートを組み込み、極低電圧の CMOS 回路を用いて動作の検証を行った。その評価結果について報告する。

キーワード　確率共鳴, ゆらぎ, しきい論理, 非同期回路, 極低電力, 素子バラツキ

Design of Basic Asynchronous Logic Circuits based on Noise-Assisted Threshold Logic

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Abstract　Device mismatches (and hence unintended operations of) of electrical circuits become apparent upon decreasing power-supply voltage of electrical circuits to reduce their power consumption, or building large-scale circuits with coarse-grained nano electronic devices. In this report, we propose a possible way to overcome this problem by utilizing nonlinear phenomena called *stochastic resonance* (SR). A double-well potential system is realized by a latch-style circuit, and SR in the latch circuit can alleviate unintended logical operations due to device mismatches, and can simultaneously attenuate the circuit's output fluctuations. Concretely, logic functions are built based on threshold literals, and a latch is used as the threshold element (not as a memory element). Even if the device mismatch disturbs logic elements, the latch causes correct state transition *stochastically*, by applying an optimal strength of noises to the latch. Moreover, hysteresis characteristics of the latch enables that after the correct state transition, the state will be maintained regardless of the applied noise's perturbations. Since this function is indeed caused by SR, we call the logic element **SR gate**. However, due to the stochastic nature of state transition of SR gates, one cannot expect exact timings of the transition (the time required for toggling the outputs, or more simply, delay time of SR gates). Therefore, we employ design methodology of delay-insensitive asynchronous circuit, which is referred to as the Huffman circuit, and evaluate one of the Huffman circuit built with our SR gates consisting of ultra-low-voltage CMOS devices. In this report, we exhibit the evaluated results.

Key words　Stochastic resonance, noise, threshold logic, asynchronous circuits, low power, device mismatch

1. Introduction

The effect of stochastic resonance (SR), refers to the utilization of an optimal amount of noise to improve specific tasks [1]. One of the main applications of the SR effect is the improvement of the response of nonlinear systems to subthreshold inputs [2]. Recently, a novel application of noise in nonlinear systems was proposed by Murali *et al.*, where a certain range of noise serves to change the state in a bistable system; each state represents a logic state, and therefore the basic logic operations can be implemented by electrically modeling a double-well potential function with an additive Gaussian noise [4]; further, the precise values for the bias are necessary to set the logical operation, and this requires additional bias sources. Moreover, the implementation of this system is quite complex because it requires the use of several operational amplifiers and additional bias circuits, which is expensive in terms of VLSI. It has been also proposed to select each logic function by tuning the amount of noise, which is impractical for real applications. This paper proposes a novel configuration, by cooperative use of noise in nonlinear systems. This work presents two main advantages. One is the possibility of working with ultra low power supply, due to the fact that the utilization of noise allows an indirect modification of threshold voltages. The second one, is that the concept involves electrical systems where the hysteresis phenomenon occurs. In this case, the presence of two thresholds prevents the activation of the output in the presence of large noise fluctuations. However, a main limitation is the unpredictable transition time of the SR gates. The delay time of the SR gate response is limited by the stochastic process; therefore, synchronization is the main limitation for the effective performance of high-complexity circuit configurations. However, a suitable alternative is the implementation of asynchronous circuits with the current SR gates, considering the lack of a common clock. This characteristic allows a more reliable design of the elements in the presence of delays, such as in the SR gate case. Further, the performance of the SR logic in a sequential asynchronous design has been demonstrated.

The reminder of this paper is organized as follows, Section 2 presents a description of the main idea of this work to design the stochastic resonance logic gates. Section 3 presents the electrical simulations of the proposed circuit. Section 4 presents the simulation of one of the basic asynchronous models, the Huffman model, to demonstrate the performance of the current SR gates. Finally, Section 4 presents the conclusions of this work

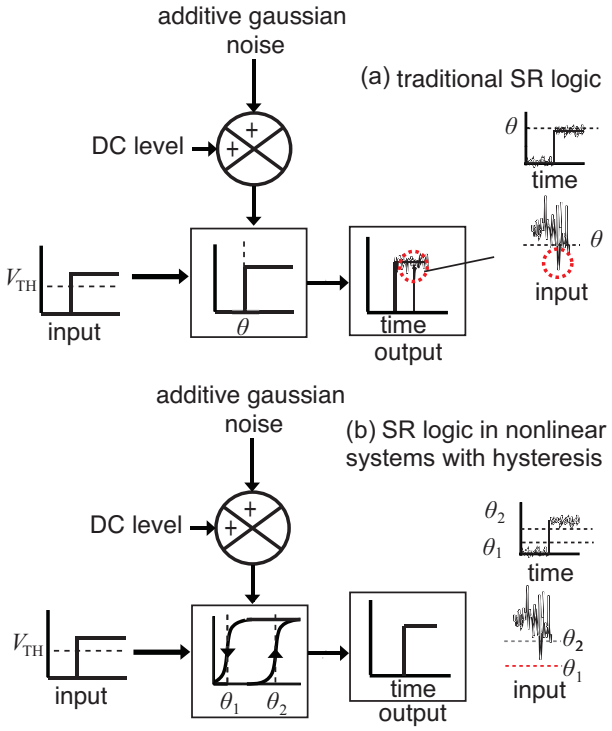

Figure 1 (a) Traditional SR logic, (b) SR logic in nonlinear systems with hysteresis

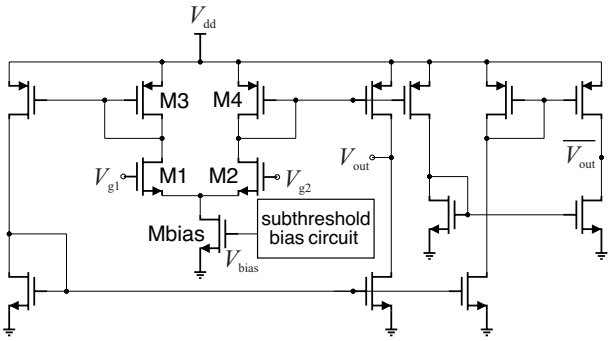

Figure 2 Electrical circuit of the SR nand gate

2. Stochastic resonance in double threshold systems

The idea of this paper is based on the utilization of noise to build logic gates. The main design is based on electrical systems with hysteresis, which posses a double threshold. Traditionally, noise assistance has been used to improve subthreshold signals detection in systems with one threshold. However, one evident problem is that a high or low amplitude peak of the noise signal could trigger an unnecessary response (Fig. 1a). In this case, the response will have fluctuations and hazards; In our case, the double-threshold system avoids hazards. When the input is lower than the threshold θ_1, the system state will change to zero; in this case to change the state to 1, the input must exceed the threshold θ_2 instead of threshold θ_1. Here, the value of the threshold

θ_2 is larger than the one of threshold θ_1; this actually will help to maintain the state of the system stable, even in the presence of large fluctuations of noise.

Figure 2 shows the proposed electrical diagram of the implementation of the SR gates. This configuration is a differential pair configuration where V_{g1} and V_{g2} denote the floating gates, and V_{out} and $\overline{V_{out}}$ are the outputs. V_{bias1} and V_{bias2} serve as selectors for the logic operations. The main concept is to indirectly vary the threshold of the transistors through an external bias. When the threshold varies, the input voltage required to activate the transistor of the differential pair, also varies. The generic symbol of a four-terminals SR gate is shown in Fig. 3. Table 1 lists the combinations of V_{bias1} and V_{bias2} to set either the NOR or the NAND operation with V_{out} as the output. By selecting $\overline{V_{out}}$ as the output, both the OR and the AND operations can be performed (Fig. 4). All the inputs of the differential pair are capacitively coupled, such as a floating gate MOSFET, and therefore the floating potential is the result of the weighted sum of their inputs. The introduction of noise (V_{noise}) aids in the detection of the weak input signals as well as to overcome the problem associated with the mismatch between the threshold voltages.

3. Simulations and results

The circuit simulations are performed through a SPICE program using a 0.18μm CMOS technology. The power supply is set to 0.35 V and all the transistors are working in the subthreshold region. Additive Gaussian noise is introduced in V_{noise} with a mean value of 0, a standard deviation of 18mV and an offset voltage of V_{dd}. The SR effect is observed during simulations. For low values of standard deviation of noise, inputs do not exceed the threshold and there is no response; for high values of the standard deviation of noise, the circuit has unwanted spikes.

One well-known advantage of the subthreshold regimen is the reduction of the power consumption; however one implication, is the increase of the sensitivity of the threshold-voltage variations; particularly in the differential pair configuration, where a precise matching is required between the transistors. In this case, the introduction of noise actually helps to overcome this problem. During the simulations, the threshold voltage of M2 was intentionally varied by modifying it directly from its SPICE transistor model. Figure 5 shows the simulation results of the SR gates of the four basic logic gates.

4. Design of asynchronous circuits based on the SR gates

As mentioned in Section 2, the response of the stochastic

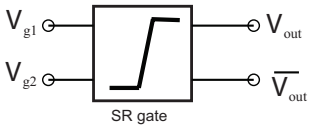

Figure 3 Symbol of a generic SR gate with no positive feedback

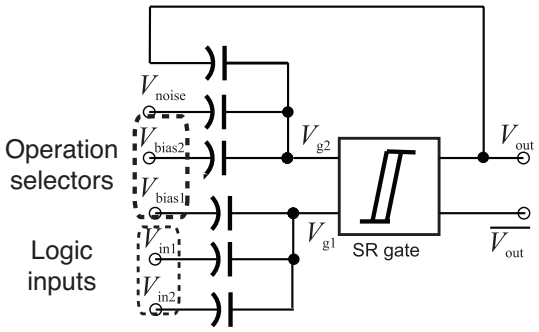

Figure 4 Symbol of a generic SR gate

Table 1 Selection of the logic operations according to V_{bias1} and V_{bias2}, and V_{out} and $\overline{V_{out}}$

V_{bias1}	V_{bias2}	$\overline{V_{out}}$	V_{out}
V_{dd}	0	OR	NOR
V_{dd}	V_{dd}	AND	NAND

Figure 5 Simulation results for the SR NOR, OT, AND and NAND gates

logic gates is governed by the stochastic processes; therefore, the delay time of the SR gate response tends to be unpredictable for a certain time period. This timing limitation is crucial in circuits sharing a common clock, such as the synchronous circuits. In synchronous circuit designs, a precise synchronization among the signals must exist to ensure an effective performance. Therefore, SR gates find suitable applications in asynchronous circuits. The main characteristic of the asynchronous circuits is the use of handshaking among the circuit stages to achieve synchronization, to communicate with each other, and to complete all the tasks. Basically, by using the asynchronous logic, it is possible to model the existence of delays in the circuit elements. Such is the case of the Huffman asynchronous circuit model, which considers a bounded delay [0,U] for each element. This allows reliable

Figure 6 Diagram block of the winery-shop-patron problem

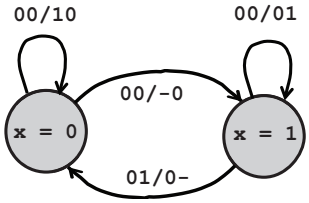

Figure 7 Asynchronous finite-state machine (AFSM) diagram for the winery-shop-patron problem

circuit designs even in the presence of delays.

A simple sequential circuit design is presented in this paper, to prove the effective performance of the SR gates. This circuit design is based on the problem presented in [5], referring as the winery-shop-patron problem (Fig. 6), where the statement is as follows, the wine shop must request for wine to the winery (this action is denoted by the signal `req_wine`); once the wine arrives at the shop (the acknowledging of that request is denoted by `ack_wine`), the patron is called to pick the wine up (denoted by `req_patron`). Once the patron arrives to pick the wine up (acknowledging the request, denoted `ack_patron`), the process is complete. As shown in Fig. 6, the arrows denote the channels communications.

As the "shop" is responsible for both the request (to the winery and the patron), it is said that the "shop" is an active/active protocol. A common representation of these models is through asynchronous finite-state machine (AFSM) diagram (Fig. 7). The circles denote the state and the arrows denote the transitions. It can be noted that a new variable state, `x` is introduced in order to reduce the number of states. The corresponding digital circuit can be obtained by Karnaugh map reduction. The implementation of the circuit is shown in Fig. 8, using the traditional logic gates. It can be noted that in this circuit, the delay elements are considered for all the components. In this case, any lack of desynchronization among the signals can be compensated by adding a feedback between the variables `x` and `X`. This feedback must contain the delay elements whose delay time is sufficient large to compensate for the internal delays.

Figure 9 shows the implementation of the active/active protocol by using the SR gates. In this circuit, the buffer can be implemented by using the same configuration as that of the SR-NAND with both the inputs connected to the same input. Similarly, a buffer can be implemented by using an SR AND, with one terminal connected to the logic 1. The

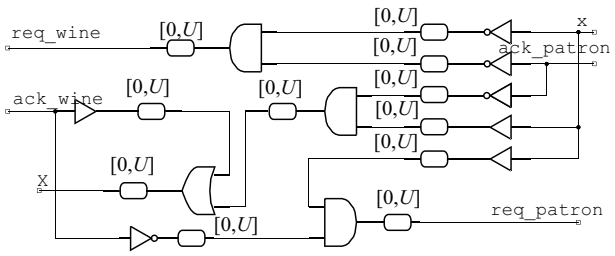

Figure 8 Logic gate representation of the winery-shop-patron problem, based on the Huffman model

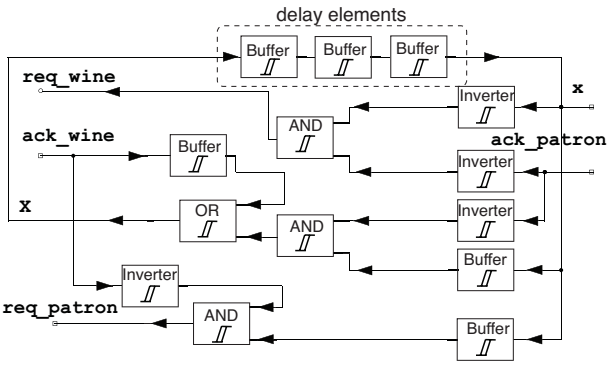

Figure 9 SR gate representation of the winery-shop-patron problem

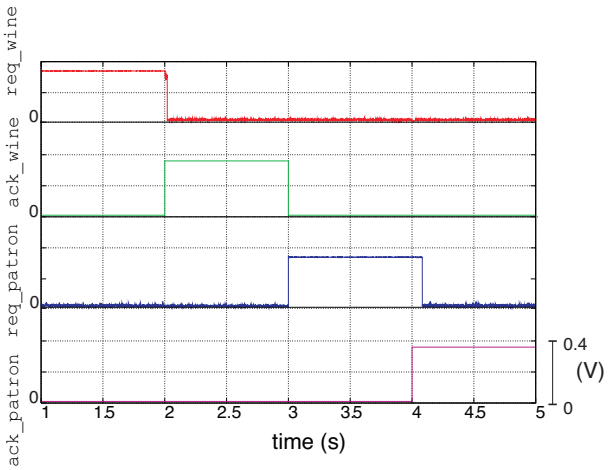

Figure 10 simulation results of the winery-shop-patron circuit

simulation results are shown in Fig. 10, where the sequence of the winery problem is correctly performed.

5. Conclusion

The SR effect has been demonstrated to be an effective technique to detect weak stimuli in nonlinear systems. The main contribution of this study is the use the hysteresis characteristic of the differential pair configuration to avoid spontaneous hazards and high amplitude oscillations. Moreover, the proposed circuit can be used to implement the four basic logic gates, by simply varying the two external bias values, either to 0 or to V_{dd}. Owing to the fact that all the transistors are working in the subthreshold regime, the circuit achieves a

low power consumption. According to the electrical simulations, power consumption is in the order of $\sim pW$. However a formal power and speed analysis will be done in further works for more complex configurations. Also the introduction of noise actually reduces the mismatch effect. The circuit simulations have demonstrated the effectiveness of using noise in the proposed configuration to build logical circuits. As a future work, asynchronous circuits with a higher level of complexity will be simulated by using the SR gates as a main element.

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