

# Reaction-Diffusion Computers on Semiconductors

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This paper presents an overview of the semiconductor implementation of reaction-diffusion (RD) computers in large-scale integrated (LSI) circuits [1]. There, we show how to model RD processes in LSI circuits and discuss several designs of RD digital chips, based on cellular-automaton models of RD and excitable systems. Feasibility of a RD digital chip is demonstrated in the construction of a Voronoi diagram and decomposition of images. The report concludes with analogue RD chips, where closer to physical reality nonlinear characteristics of chemical systems are employed. We propose designs of RD chips based on Oregonator, Turing and so on. We exemplify functionality of analogue RD chips in edge detection, feature extraction and fingerprint reconstruction tasks.

## 1. Introduction

What is a reaction-diffusion (RD) processor? A traditional RD processor is a real ‘liquid’ medium, usually composed of a thin layer of solution or gel containing chemical reagents, that in its space-time dynamics transforms data to results in a sensible and programmable way. Data, to be processed, can be represented by the concentration of certain reagents and spatial structures, e.g., diffusive or excitation waves, spread from these initial data points. The spreading patterns interact to produce either stationary structures, e.g., a precipitate concentration profile, or dissipative structures, e.g., oscillating patterns. The final state, or even just a particular spatial state of the whole medium, represents a result of the RD computation.

The spreading of waves is analogous to information transfer. And, the interaction of diffusive or phase waves realises the computation. An important attribute of this mode of computation is that there is an absence of a rigid hardware-like structure. Essentially, the ‘liquid’ processor has an ‘amorphous’ structure which may be considered as a layer of micro-volume RD chemical processors capable of massive parallelism. Characteristic advantages of RD processors include parallel input of data (usually, via the spatial distribution of the reactant concentrations), massively parallel information processing (typically, via spreading and interaction of either phase or diffusive waves) and parallel output of results of the computation (commonly, the results are represented by patterns of reactants or a coloured precipitate that enables the use of optical reading devices). These features together with the relative ease of laboratory experiments (most reactions occur at room temperature and do not require any specialist equipment), constructional simplicity of formal design (all RD systems are well simulated in two-dimensional cellular automata) and the pleasure of parallelism per se make RD chemical processors an invaluable tool for developing advanced unconventional parallel computing architectures.

Recently, a great deal of attention has been paid to the study of the computational properties of spatially extended chemical systems. To date, it has been proved experimentally that RD chemical processors are capable of computing shortest paths, image processing, computational geometry, pattern recognition and logical computation. In the last ten years enough results have been obtained to demonstrate that RD chemical processors are not simply curiosities invented by theoreticians but promising — and somewhat revolutionary — computing architectures offering an alternative to the as yet unchallenged domination of the current silicon designs. This is because spatially extended RD processors are equivalent to massively parallel computers.

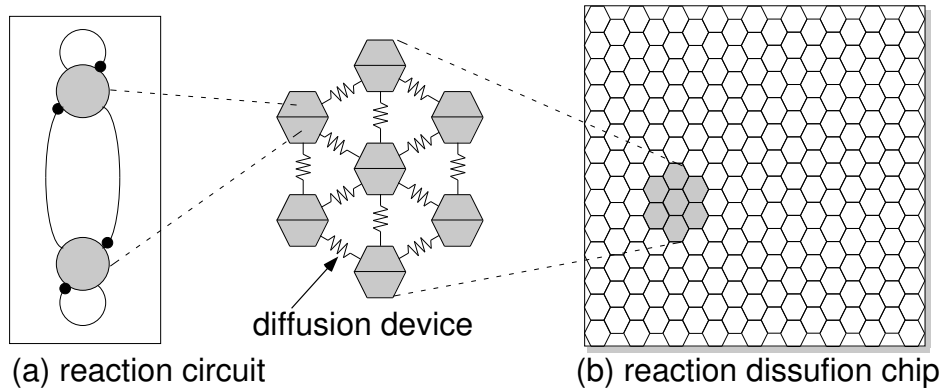


Figure 1: Basic construction of RD chip.

A two-dimensional RD processor, implemented in a thin-layer liquid phase in a Petri dish, consists of millions of micro-volumes, nearly  $10^{19}$ . The concentrations of reactants in each micro-volume are changed in parallel depending on reagent concentrations in neighbouring micro-volumes. Therefore, a thin layer of a chemical medium could be seen as an (ir)regular array of elementary few-bit processors. The great number of elementary processing units makes chemical computers tolerant to impurities of RD media while local connectivity allows for localisation of spatial inhomogeneities in the reacting medium. The ‘amorphous’ structure of the chemical medium guarantees that a massively parallel chemical processor will self-reconfigure and restore its original architecture after some parts of the physical processing medium are removed.

This paper introduces so-called *reaction-diffusion chips* [1] implementing these RD processors. A RD chip consists of i) reaction circuits that emulate elementary interactions between neurons (or chemical substances) and ii) diffusion devices that imitate synapses (or chemical diffusion of the substances). Figure 1(a) shows a schematic image of self- and mutual-interactions (reactions) between two neurons (chemical substances). The reaction circuit is arranged on a hexagonal grid [Fig. 1(b)] and is connected with its neighboring circuits through the diffusion devices. RD chips were mostly designed by digital, analog, or mixed-signal complementally metal-oxide-semiconductor (CMOS) circuits of cellular neural networks (CNNs) or cellular automata (CA). Electrical cell circuits were designed to implement several CA and CNN models of RD systems [2, 3, 4, 5], as well as fundamental RD equations [6, 7, 8, 9, 10]. Each cell is arranged on a 2D square or hexagonal grid and is connected with adjacent cells through coupling devices that transmit a cell’s state to its neighboring cells, as in conventional CAs. For instance, an analog-digital hybrid RD chip [3] was designed for emulating a conventional CA model for BZ reactions [11]. A precipitating BZ system for computation of Voronoi diagram [12, 13] was also implemented on an analog-digital hybrid RD chip [5]. A full-digital RD processor [4] was also designed on the basis of a multiple-valued CA model, called *excitable lattices* [14]. Furthermore, a RD CA processor for complex image processing has been proposed [15]. It performs quadrilateral-object extraction based on serial and parallel CA algorithms. An analog cell circuit was also designed to be equivalent to spatial-discrete Turing RD systems [8]. A full-analog RD chip that emulates BZ reactions has also been designed and fabricated [7]. Furthermore, blue-prints of non-CMOS RD chips have been designed; i.e., a RD device based on minority-carrier transport in semiconductor devices [6]. In the following sections, we see how to construct an artificial RD system on *solid-state media* (silicon), and to develop some applications using the solid-state RD system that could cope with conventional digital computers.

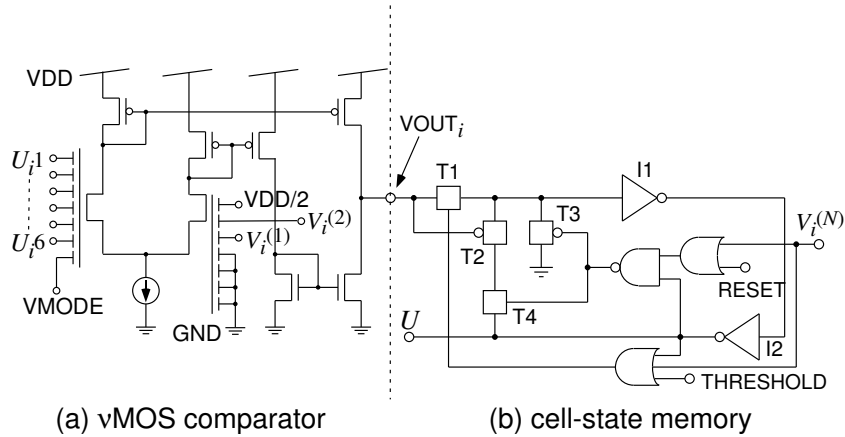


Figure 2: Cell circuit for transition decision [3].

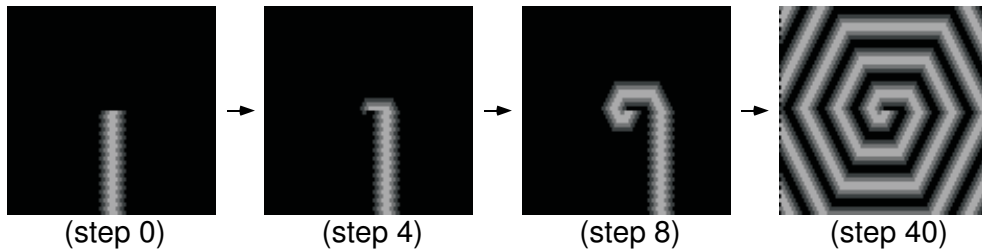


Figure 3: Excitatory modelock operations of RD circuit [3].

## 2. Digital CMOS Reaction-Diffusion Chips

### 2.1 A reaction-diffusion circuit based on cellular-automaton processing emulating the Belousov-Zhabotinsky reaction

The Belousov-Zhabotinsky (BZ) reaction provides us important clues to control 2D phase-lagged stable synchronous patterns in excitable medium. Because of the difficulty in computing RD systems in large systems using conventional digital processors, we proposed a cellular-automaton (CA) circuit that emulates the BZ reaction [3]. In the circuit, a two-dimensional array of parallel processing cells, shown in Fig. 2, is responsible for the emulation, and its operation rate is independent of the system size. We demonstrated the operations of the proposed CA circuit, by using a simulation program with integrated circuit emphasis (SPICE). In the circuit's initial state, cells adjacent to inactive cells were in a refractory period (step 0 in Fig. 3). The inactive cells adjacent to the white bar in Fig. 3 were suppressed by adjacent cells in the refractory period (cells in the white bar). The inactive cells then entered an active, inactive, or refractory period, depending on the degree of the refractory condition. When the inactive cells were in an active or inactive period, the tip of the bar rotated inward (step 4 to 8 in Fig. 3), resulting in the generation of the modelock (spiral patterns) typically observed in the BZ reaction (step 40 in Fig. 3). A hexagonal distortion of the propagating waves was generated by interactions between adjacent cells. These results indicated that the proposed RD chip could be easily integrated into existing digital systems and can be used to clarify RD systems, aiming at developing further novel applications.

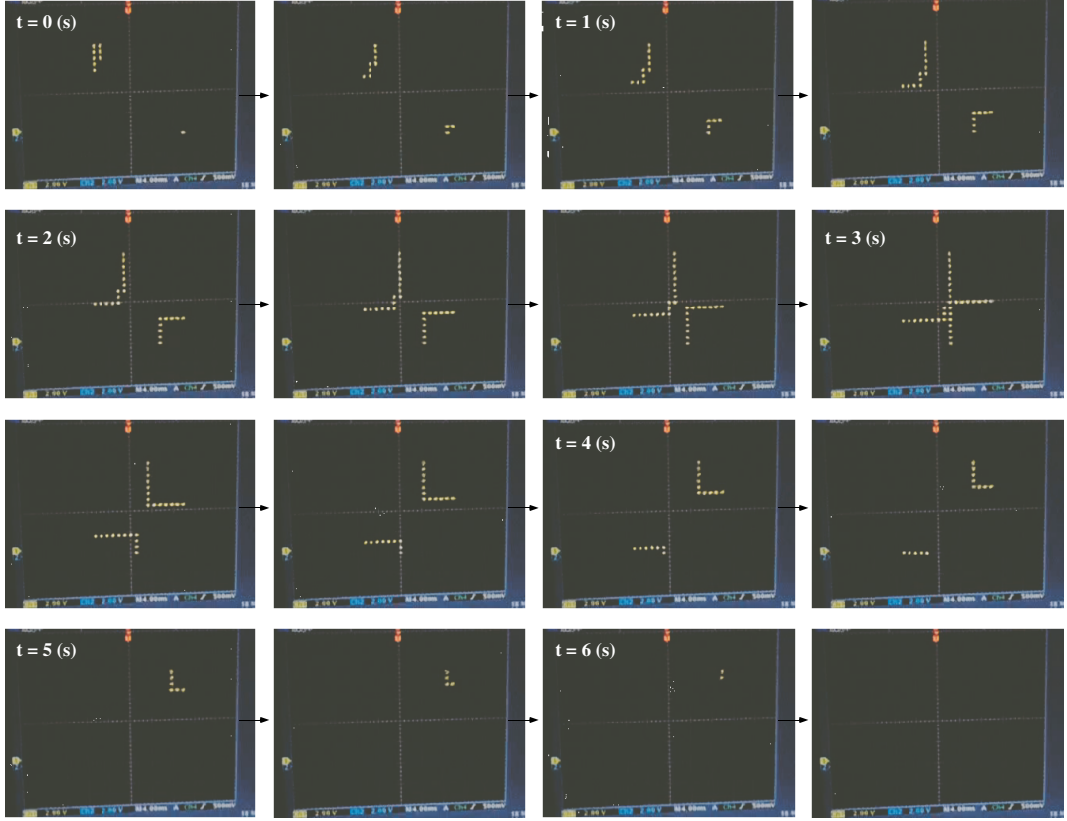


Figure 4: Snapshots of recorded movie obtained from fabricated RD chip [4].

## 2.2 Reaction-diffusion chip implementing excitable lattices with multiple-valued cellular automata

We fabricated a RD chip based on a multiple-valued CA model of excitable lattices [4]. Our experiments confirmed the expected operations, i.e., excitable wave propagation and annihilation. We could obtain a binary stream from the common output wire by selecting each cell sequentially. Using a conventional displaying technique, the binary stream was reconstructed on a 2-D display. Figure 4 shows the movie we recorded. Each dot represents an excitatory cell where EXC is logical “1”. In the experiment, the supply voltage were set at 5 V, and the system clock was set at low frequency (2.5 Hz) so that “very-slow” spatiotemporal activities could be observed visually (the low frequency was used only for the visualization, and was not the upper limit of the circuit operation). We applied pin-spot lights to several cells at top-left and bottom right corners of the chip. The circuit exhibited the expected results; i.e., two excitable waves of excited cells triggered by the corner cells propagated toward the center and disappeared when they collided. This result suggests that if we use a more microscopic process and a large number of cells were implemented, we would observe the same complex (BZ-like) patterns, as observed in the original excitable lattices [14].

This chip can operate much faster than real chemical RD systems, even when the system clock frequency is  $O(1)$  Hz, and is much easier to use in various experimental environments. Therefore, the chip should encourage RD application developers who use such properties of excitable waves to develop unconventional computing schemes, e.g., chemical image processing, pattern recognition, path planing, and robot navigation.

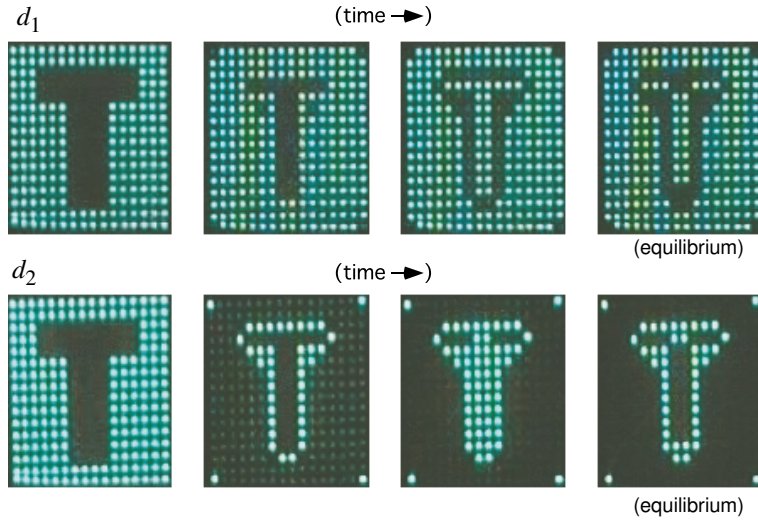


Figure 5: Skeleton operation with “T” shape [5].

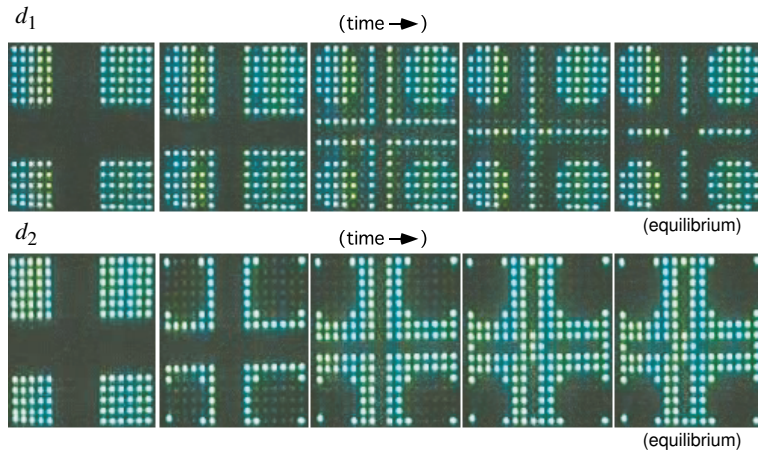


Figure 6: Skeleton operation with “+” shape [5].

### 2.3 Silicon implementation of a chemical reaction-diffusion processor for computation of Voronoi diagram

RD chemical systems are known to realize sensible computation when both data and results of the computation are encoded in concentration profiles of chemical species; the computation is implemented via spreading and interaction of either diffusive or phase waves, while a silicon RD chip is an electronic analog of the chemical RD systems.

We have developed a prototype RD chip implementing a chemical RD processor for a well-known NP-complete problem of computational geometry — computation of a Voronoi diagram. We offered experimental results for fabricated RD chips and compare the accuracy of information processing in silicon analogs of RD processors and their experimental ‘wetware’ prototypes [5]. Figures 5 and 6 show examples of skeleton operation of a T and ‘+’ shaped images. As initial images, we make a glass mask where ‘T’ and ‘+’ areas are exactly masked. Therefore, cells under the ‘T’ and ‘+’ areas are initially resting and the rest are initially excited. At its equilibrium, skeletons of ‘T’ and ‘+’ were successfully obtained.

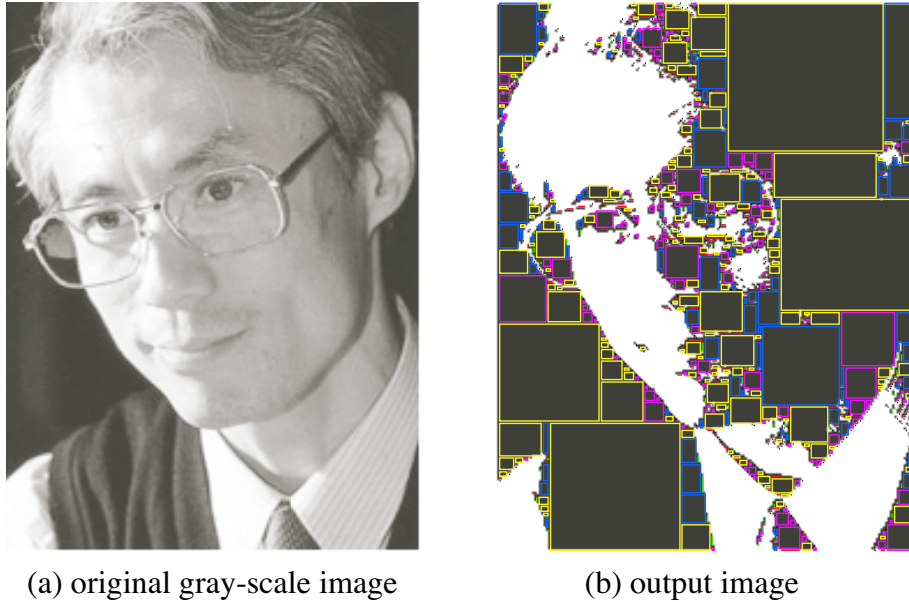


Figure 7: Simulation results for  $181 \times 238$  image; (a) original image, (b) mixed image of quantized image given to CA LSI and detected quadrilateral objects [15].

#### 2.4 A quadrilateral-object composer for binary images with reaction-diffusion cellular automata

We proposed a CA LSI architecture that extracted quadrilateral objects from binary images [15]. We proposed a serial combination of parallel CA algorithms, based on RD chemical systems model. Each cell in the CA was implemented by a simple digital circuit called an elemental processor. The CA LSI can be constructed by a large number of elemental processors and their controllers operating in serial and parallel.

Figure 7(a) demonstrates object extraction for a natural image. The image was quantized, and given to the CA LSI. Figure 7(b) show the results. The maximum boxes were correctly detected in order, as predicted. The input bitmap image that consisted of  $181 \times 238$  pixels was decomposed of 1,020 quadrilateral objects. The bitmap image occupied 43,078 bits (5,385 bytes) on memory, while the objects used 4,080 bytes (8-bit address of 4 corners  $\times$  1,020 boxes). The important thing is not discussing the compression rate between bitmap images and extracted objects, but that bitmap images were represented by small number of vector objects, which facilitates picture drawing in terms of the drawing speed if we have variable box window.

One of the most important application targets for the proposed chip is a computer-aided design (CAD) system for VLSIs. Conventional VLSI CAD tools use polygons to represent device structures. However, recent VLSIs include not only polygon patterns but also graphical patterns, consisting of large number of dots, usually imported from image files such as JPEGs, to implement complex analog structures. In the mask manufacturing process, exposing a large number of dot patterns is quite a time-consuming task. Recently, electron beam (EB) lithography systems that can expose wide areas through a quadrilateral window have been produced on a commercial basis. The proposed LSI can produce efficient stream files from binary image files that can easily be handled by the new EB systems, by developing simple software that converts the box format, produced by the proposed LSI, to a conventional stream format.



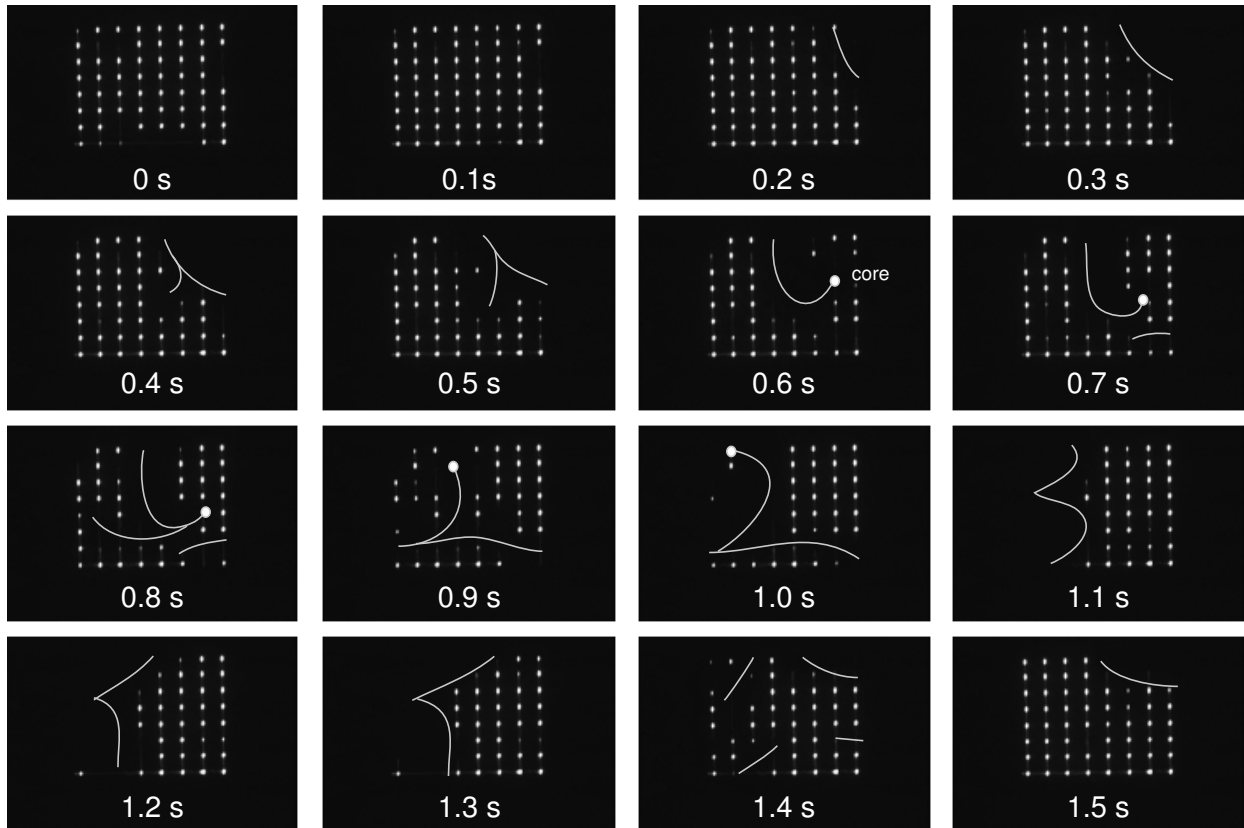


Figure 8: Spiral patterns on RD chip (weak connections between cells) [7].

### 3. Analog CMOS Reaction-Diffusion Chip

#### 3.1 Analog reaction-diffusion chip with Hardware Oregonator Model

Silicon devices that imitate the autocatalytic and dissipative phenomena of RD systems were developed [7]. Numerical simulations and experimental results revealed that an RD device could successfully produce concentric and spiral waves in the same way as natural RD systems. These results encouraged us to develop new applications based on natural RD phenomena using hardware RD devices.

Figure 8 presents an example where some spiral (modelock) patterns of cell clusters were observed. Snapshots were taken with at intervals of 100 ms. The active-cell clusters and cores of the spirals are superimposed with the figure by white curves and white circles, respectively. Although observing “beautiful” spirals as in chemical RD systems is difficult because of the small number of cells, the appearance and disappearance of small sections of spiral waves were successfully observed.

RD devices and circuits are useful not only for hardware RD systems but also for constructing modern neuro-chips. The excitatory and oscillatory behaviors of an RD device and circuit are very similar to actual neurons that produce sequences of identically shaped pulses in time, called *spikes*. Recently, Fukai demonstrated that an inhibitory network of spiking neurons achieves robust and efficient neural competition on the basis of a novel timing mechanism of neural activity. A network with such a timing mechanism may provide an appropriate platform to develop analog VLSI circuits and could overcome problems with analog devices, namely their lack of precision and reproducibility.

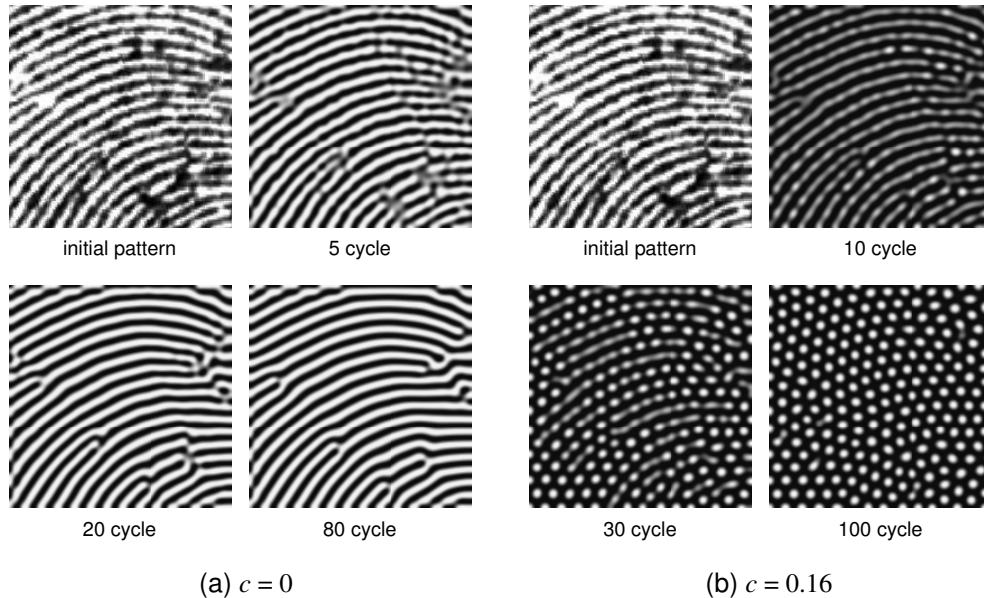


Figure 9: Snapshots of pattern formation from initial fingerprint image [17].

### 3.2 Striped and spotted pattern generation on RD cellular automata

We proposed a novel RD model that is suitable for LSI implementation and its basic LSI architecture [17]. The model employs linear diffusion fields of activators and inhibitors and a discrete transition rule after diffusion. We developed image-processing LSI circuits based on pattern formation in RD systems. We introduced continuous diffusion fields and an analog state variable to Young's local activator-inhibitor model [18]. We produced a model pattern diagram on a 2D parameter space through extensive numerical simulations. We showed that the spatial frequency and form (striped or spotted) could be controlled with only two parameters. Theoretical analysis of the one dimensional model proved that i) spatial distribution given by a periodic square function is stable at the equilibrium and ii) the spatial frequency is inversely proportional to the square root of a diffusion coefficient of the inhibitors.

We designed a basic circuit for the proposed model. We designed an RD LSI based on the analog computing method where the concentration of chemicals was represented by a 2D voltage distribution and the cell voltage was diffused step by step. By mimicking two diffusion fields with the proposed model in one diffusion circuit on the LSI, we reduced the area of the unit cell circuit.

Figure 9(a) has snapshots of pattern formation in the circuit. We could estimate that the system produces striped patterns from our theory [17]. Therefore, we used a fingerprint pattern as an initial input. We confirmed that noisy local patterns were repaired by their surrounding striped patterns, as time increased. The circuit required 50 cycles (8000 clocks) to reach equilibrium. Figure 9(b) shows the results for spot pattern generation. The same initial input as in Fig. 9(a) was given to the circuit. As expected from our theory, spotted patterns were obtained. The pattern formation process was the same as in Fig. 9(a) where noisy local spots were restored by surrounding global spotted patterns. Therefore, this circuit would be suitable for restoring regularly-arranged spotted patterns such as polka-dot patterns. The system took 100 cycles (16,000 clocks) until it reached equilibrium to restore the spotted patterns.



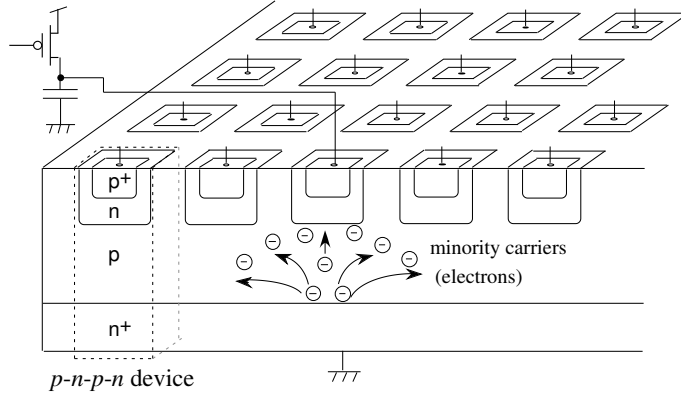


Figure 10: Construction of two-dimensional RD device with vertical  $p-n-p-n$  device [6].

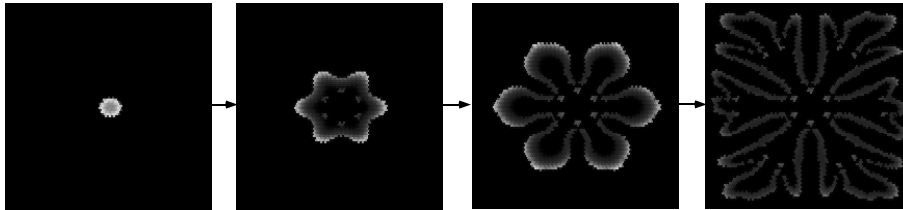


Figure 11: Simulation results of RD device producing multiplying patterns. [6].

#### 4. Reaction-diffusion computing devices based on minority-carrier transport in semiconductors

We proposed a massive parallel computing device [6] based on principles of information processing in RD chemical media [19, 14] (Figs. 10 and 11). This device imitates auto-catalytic and dissipative phenomena of the chemical RD systems, however comparing to real chemical medium the semi-conductor analog of RD computers, functions much faster. We studied operational characteristics of the RD silicon devices and demonstrate feasibility of the approach on several computational tasks. Our results indicate that the proposed RD device will be a useful tool for developing novel hardware architectures based on RD principles of information processing.

Practical value of RD chemical systems are significantly reduced by low speed of traveling waves which makes real-time computation senseless. One of the cost-efficient options to overcome the speed-limitations of RD computers while preserving unique features of wave-based computing is to implement RD chemical computers in silicon. The velocity of traveling wavefronts in typical reaction diffusion systems, e.g., BZ reaction, is  $10^{-2}$  m/s [20], while that of a hardware RD system will be over a million times faster than that of the BZ reaction, independent of system size [1]. The increase in speed will be indispensable for developers of RD computers. Moreover, if a RD system is implemented in integrated circuits, then we would be able to artificially design various types RD spatio-temporal dynamics and thus develop parallel computing processors for novel applications. Basing on experimental evidences of RD-like behaviour, namely traveling current density filaments [21], in  $p-n-p-n$  devices we propose a novel type of semiconductor RD computing device, where minority carriers diffuse as chemical species and reaction elements are represented by  $p-n-p-n$  diodes.

## 5. Collision-based RD Computers

Present digital VLSI systems consist of a number of combinational and sequential logic circuits as well as related peripheral circuits. A well-known basic logic circuit is a two-input NAND circuit that consists of four metal-oxide semiconductor field-effect transistors (MOS FETs) where three transistors are on the current path between the power supply and the ground. Many complex logic circuits can be constructed by not only populations of a large number of NAND circuits but also special logic circuits with a small number of transistors (there are more than three transistors on the current path) compared with NAND-based circuits.

A straight-forward way to construct low-power digital VLSIs is to decrease the power-supply voltage because the power consumption of digital circuits is proportional to the square of the supply voltage. In complex logic circuits, where many transistors are on the current paths, the supply voltage cannot be decreased due to stacking effects of transistors' threshold voltages, even though the threshold voltage is decreasing as LSI fabrication technology advances year by year. On the other hand, if two-input basic gates that have the minimum number of transistors (three or less) on the current path are used to decrease the supply voltage, a large number of the gates will be required for constructing complex logic circuits.

The Reed-Muller expansion [22, 23], which expands logical functions into combinations of AND and XOR logic, enables us to design 'specific' arithmetic functions with a small number of gates, but it is not suitable for arbitrary arithmetic computation. Pass-transistor logic (PTL) circuits use a small number of transistors for basic logic functions but additional level-restoring circuits are required for every unit [24]. Moreover, the acceptance of PTL circuits into mainstream digital design critically depends on the availability of tools for logic, physical synthesis, and optimization. Current-mode logic circuits also use a small number of transistors for basic logic, but their power consumption is very high due to the continuous current flow in turn-on states [25]. Subthreshold logic circuits where all the transistors operate under their threshold voltage are expected to exhibit ultra-low power consumption, but the operation speed is extremely slow [26]. Binary decision diagram logic circuits are suitable for next-generation semiconductor devices such as single-electron transistors [27, 28], but not for present digital VLSIs because of the use of PTL circuits.

To address the problems above concerning low-power and high-speed operation in digital VLSIs, we describe a method of designing logic circuits with collision-based fusion gates, which is inspired by collision-based RD computing (RDC) [29, 1]. In the following sections, we introduce a new interpretation of collision-based RDC, especially concerning directions and speeds of propagating information quanta. We also show basic logical functions constructed by collision-based fusion gates, and discuss the number of transistors in classical and fusion-gate logic circuits [30, 31].

### 5.1 Collision-Based Reaction-Diffusion Computing for digital VLSIs

Adamatzky proposed how to realize arithmetical scheme using wave fragments traveling in a RD medium where excitable chemical waves disappear when they collide each other [29, 1]. His cellular-automaton model mimicked localized excitable waves (wave fragments) traveling along columns and rows of the lattice and along diagonals. The wave fragments represented values of logical variables where logical operations were implemented when wave fragments collided and were annihilated or reflected as a result of the collision. One can achieve basic logical gates in the cellular-automaton model, and build an arithmetic circuit using the gates [29].

The cellular-automaton model for basic logic gates has been implemented on digital VLSIs [1]. Each cell consisted of several tens of transistors and was regularly arranged on a 2D chip surface. To implement a one-bit adder, for example, by collision-based cellular automata, at least several tens of cells are required to allocate sufficient space for the collision of wave fragments [29]. This implies several hundreds of transistors are required for constructing just a one-bit adder. Direct

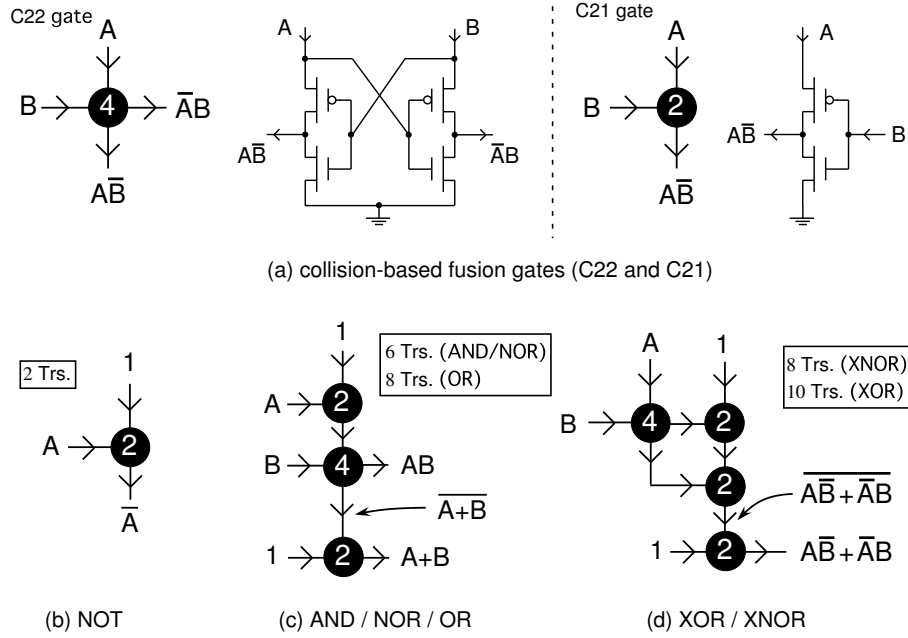


Figure 12: Construction of collision-based fusion gates [30, 31]. (a) Definition of 2-in 2-out (C22) and 2-in 1-out (C21) gates and their corresponding circuits; (b) NOT; (c) AND, NOR, and OR; (d) XOR and XNOR functions.

implementation of the cellular automaton model is therefore a waste of chip space, as long as the single cell space is decreased to the same degree of chemical compounds in spatially-continuous RD processors.

What happens if wave fragments travel in ‘limited directions instantaneously’? Our possible answers to this question are depicted in Figure 12. Figure 12(a) shows our 2-in 2-out (C22) and 2-in 1-out (C21) units representing two perpendicular ‘limited’ directions of wave fragments, i.e., North-South and West-East fragments. The number of MOS transistors in each unit is written inside the black circle in the figure. The input fragments are represented by values A and B where A (or B) = ‘1’ represents the existence of a wave fragment traveling North-South (or West-East), and A (or B) = ‘0’ represents the absence of wave fragments. When A = B = ‘1’ wave fragments collide at the center position (black circle) and then disappear. Thus, East and South outputs are ‘0’ because of the disappearance. If A = B = ‘0’, the outputs will be ‘0’ as well because of the absence of the fragments. When A = ‘1’ and B = ‘0’, a wave fragment can travel to the South because it does not collide with a fragment traveling West-East. The East and South outputs are thus ‘0’ and ‘1’, respectively, whereas they are ‘1’ and ‘0’, respectively, when A = ‘0’ and B = ‘1’. Consequently, logical functions of this simple ‘operator’ are represented by  $\bar{A}B$  and  $A\bar{B}$ , as shown in Fig. 12(a) left. We call this operator a collision-based ‘fusion gate’, where two inputs correspond to perpendicular wave fragments, and one (or two) output represents the results of the collision (transparent or disappear) along the perpendicular axes. Figures 12(b) to (d) represent basic logic circuits constructed by combining several fusion gates. The simplest example is shown in Fig. 12(b) where the NOT function is implemented by a C21 gate (2 transistors). The North input is always ‘1’, whereas the West is the input (A) of the NOT function. The output appears on South node ( $\bar{A}$ ). Figure 12(c) represents a combinational circuit of three fusion gates (two C21 gates and one C22 gate) that produces AND, NOR, and OR functions. Exclusive logic functions are produced by three (for XNOR) or four (for XOR) fusion gates as shown in Fig. 12(d). The number of transistors for each function is depicted in the figure (inside the white boxes).

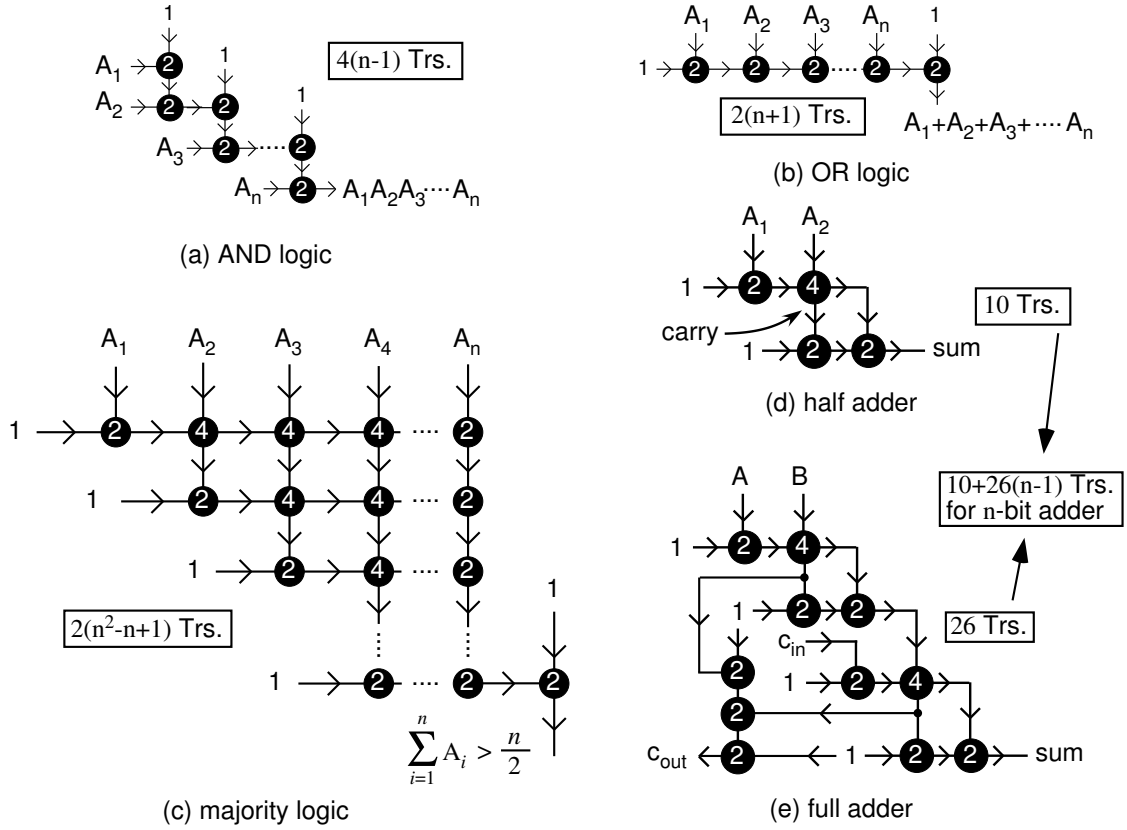


Figure 13: Fusion gate architectures of multiple-input functions [30, 31]; (a) AND, (b) OR, (c) majority logic gates. Half and full adders are shown in (d) and (e), respectively.

A collision-based fusion gate receives two logical inputs ( $A$  and  $B$ ) and produces one (C21) or two (C22) logical outputs; i.e.,  $A\bar{B}$  for C21,  $\bar{A}B$  and  $A\bar{B}$  for C22. Unit circuits for C22 and C21 gates receive logical (voltage) inputs ( $A$  and  $B$ ) and produce these logic functions. The minimum circuit structure is based on PTL circuits where a single-transistor AND logic is fully utilized. For instance, in Fig. 12(a) right, a pMOS pass transistor is responsible for the  $\bar{A}B$  function, and an additional nMOS transistor is used for discharging operations. When the pMOS transistor receives voltages  $A$  and  $B$  at its gate and drain, respectively, the source voltage approaches  $\bar{A}B$  at equilibrium. If a pMOS transistor is turned off, an nMOS transistor connected between the pMOS transistor and the ground discharges the output node, which significantly increases the upper bound of the operation frequency. When  $A = B = '0'$ , the output voltage is not completely zero because of the threshold voltage of the MOS transistors, however, this small voltage shift is restored to logical '0' at the next input stage. Therefore additional level-restoring circuits are unnecessary for this circuit.

Figure 13 shows constructions of multiple-input logic functions with fusion gates. In classical circuits, two-input AND and OR gates consist of six transistors. As introduced in section 1, to decrease the power supply voltage for low-power operation, a small number of transistors (three or less) should be on each unit's current path. Since each unit circuit has six transistors,  $n$ -input AND and OR gates consist of  $6(n-1)$  transistors ( $n \geq 2$ ). On the other hand, in fusion gate logic [(a) and (b)], a  $n$ -input AND gate consisted of  $4(n-1)$  transistors, whereas  $2(n+1)$  transistors were used in an  $n$ -input OR gate. Therefore, in case of AND logic, the number of transistors in fusion gate circuits is smaller than that of classical circuits. The difference will be significantly expanded as  $n$  increases. Figure 13(c) shows fusion gate implementation of majority logic circuits with multiple inputs. Again, in classical circuits, the number of transistors on each unit's current

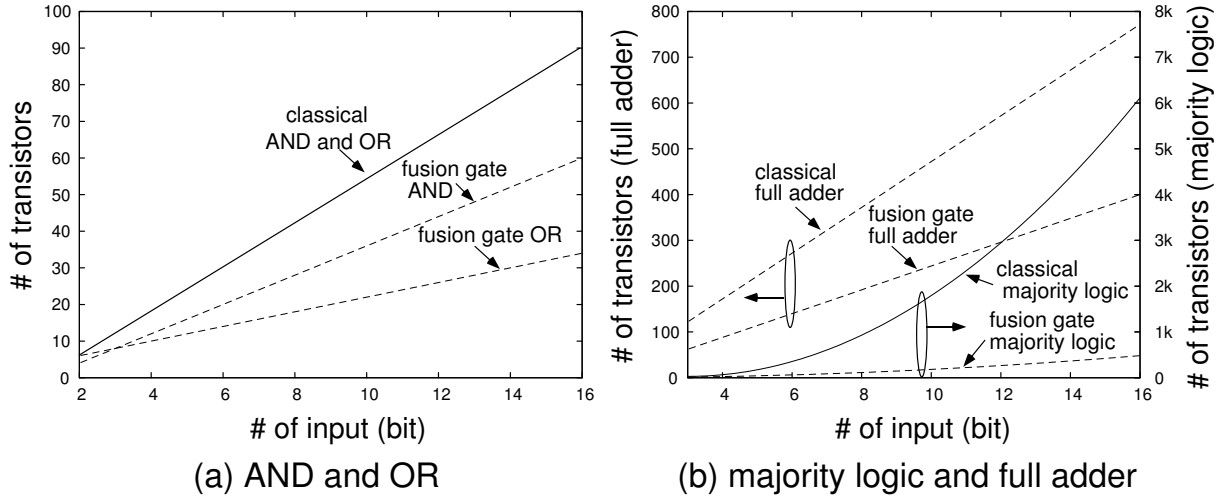


Figure 14: Total number of transistors in classical and collision-based (CB) multiple-input logic gates [30, 31].

path is fixed to three. For  $n$ -bit inputs ( $n$  must be an odd number larger than 3), the number of transistors in the classical circuit was  $30 + 36(n - 3)^2$ , while in the fusion gate circuit, it was  $2(n^2 - n + 1)$ , which indicates that the collision-based circuit has a great advantage in the number of transistors. Half- and full adders constructed by fusion gate logic are illustrated in Figs. 13(d) and (e). The number of transistors in a classical half adder was 22, while it was 10 in a fusion gate half adder [Fig. 13(d)]. For  $n$ -bit full adders ( $n \geq 1$ ), the number of transistors in a classical circuit was  $50n - 28$ , while it was  $26(n - 1) + 10$  in a fusion gate circuit [Fig. 13(e)]. Again, the fusion gate circuit has a significantly smaller number of transistors, and the difference will be increased as  $n$  increases.

Figure 14 summarizes the comparison of the number of transistors between classical and fusion gate logic. The number of transistors in fusion gate logic was always smaller than that of transistors in classical logic circuits, especially in majority logic gates.

## 6. Conclusion

Silicon devices that imitate the autocatalytic and dissipative phenomena of reaction-diffusion (RD) systems were introduced. Numerical simulations and experimental results revealed that an RD device could successfully produce concentric and spiral waves in the same way as natural RD systems. These results encouraged us to develop new applications based on natural RD phenomena using hardware RD devices.

Universal computation can be realized in RD semiconductor devices using two approaches. Firstly, by employing collision-based mode of computation in excitable media [29], where functionally complete sets of Boolean gates are implemented by colliding waves. In collision-based mode, however we must force the medium to be in a sub-excitable regime which may pose some problems from fabrication point of view. Secondly, we can ‘physically’ embed logical circuits, namely their diagram-based representations, into the excitable medium. In this we employ particulars of photo-response of RD devices and project the logical circuit onto the medium as pattern of heterogeneous illumination.

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