High-fidelity neuromorphic pulse-density modulator based on a model of vestibulo-ocular reflex

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Our purpose is to explore possible ways to construct an electrical circuit that can perform high-speed information processing with slow devices. Regarding this point, neural networks seem to be a possible choice because they are considered to perform high-speed parallel information processing with neuron elements that are relatively slower than CMOS transistors. In recent study, Hospedales *et al*. reported that a neural network with temporal noises and spatial noises in neurons that was used to perform "vestibulo-ocular reflex" (VOR) could conduct a temporal signal whose frequency was higher than operation frequency of a single neuron in networks [1]. VOR stabilizes the visual field by moving the eyeballs in such a way that compensates for rotations of the head. They reported that this function could be achieved by using temporal and spatial noises of neurons. All the neurons in the model accept common input and generate spike output i (i: neuron number). The output of the network is given by summing of outputs of all the neurons. When no noises are applied to this network, all the neurons generate spike output at the same time (phase). However, when they are affected by temporal noises ξ_i and spatial noises δ_i, they no longer can generate spike output at the same time. It represents that the network shows asynchronous firing and it can thus respond to relatively faster input signal than a single neuron.

The operation frequency in electrical circuits of a single device is limited by several conditions that derive from physical limitations. Electrical circuits are often limited by power consumption or chip area size especially in mobile appliances or sensor appliances. Information processing done by the brain is considered to have an energy-efficient structure. The architecture observed in the brain may provide possible solutions to electrical engineering. Further more, electrical-circuit engineers often try to reduce or eliminate the effects of noises and device mismatches of transistors because these effects degrade circuit characteristics and they even cause erroneous circuit operation. Typical circuit designs to reduce these effects often require additional transistors and larger transistors (= larger chips and greater power consumption), which makes it more difficult to meet the specification. Here, by implementing Hospedales *et al*.'s model in electrical circuits, noises and device mismatches in these circuits could be utilized to improve operations while group of slow devices could achieve faster operation. We constructed a simple neural-network circuit to confirm the improvements in fidelity and we then demonstrate that the operation frequency of a noisy network circuit is higher than that of a noiseless network circuit.

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References

[1] T. M. Hospedales, M. C. W. van Rossum, B. P. Graham, and M. B. Dutia, "Implications of noise and neural heterogeneity for vestibulo-ocular reflex fidelity", *Neural Computing*, 20, 3, 756–778, 2008.

[2] T. Asai, Y. Kanazawa, T. Hirose, and Y. Amemiya, "Analog reaction-diffusion chip imitating the Belousov-Zhabotinsky reaction with Hardware Oregonator Model," *International Journal of Unconventional Computing*, 1, 2, 123–147, 2005.