Towards Memristor-CMOS-Hybrid Semiconductor Devices for Neural Networks

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One of the key issues for implementing neural networks on semiconductor integrated circuits is "how we implement non-volatile analog synapses". Obviously this becomes critical if the network requires learning rules, i.e., the synaptic weights must be preserved and be updated according to the rules. Many engineers have tried to design analog synaptic devices based on existing flash-memory technologies (see e.g. [1]), but they had difficulties in designing associate controllers for electron injection and ejection as well as increasing the limited frequency of the rewriting. Recently so-called "memristor" which is the fourth basic circuit element originally introduced by Leon Chua in 1971, has been re-spotlighted since Strukov *et al.* presented the equivalent physical examples [2]. Memristive devices could naturally be exploited for implementing non-volatile synapses on electronic circuits because they are equivalent to resistors whose resistances can be held or modulated by the amount of the integrated current of them.

An abstract model system of a simple neural network for unsupervised learning using possible memristive nano-junctions has been introduced by Snider in 2007 [3]. The key idea was to employ bi-directional strategy in spike transmission on the junction, i.e., when the junction accepts a spike, a post neuron circuit returns an inverted spike to the junction, and the difference between the spike width results in the weight difference. Here we propose a practical circuit using popular semiconductor devices for integrated circuits (MOSFETs) for this abstract model, and demonstrate it on a simple perceptron, as a practical example. We then propose a new approach for a memristor-based learning circuit. Again we use MOSFETs and an abstract memristive model for bipolar resistive RAMs. The key idea is to assign a capacitor in one terminal of a memristor synapse. An input node of the memristor accepts voltage spikes, and the other node is connected to a gate terminal of a MOSFET where the node is capacitively coupled with the ground. This gate capacitor is charged or discharged by the input spike via the memristor. Because a MOSFET has nonlinear characteristics between the gate voltage and the drain current, by integrating the drain currents on the other (membrane) capacitor, we obtain different membrane potentials for different resistance of the memristor. If the membrane potential exceeds a given threshold voltage, a post neuron circuit (standard integrate-and-fire circuit) generates a voltage spike, and reset the membrane potential. At the same time, the gate node is shunted by an additional MOSFET (the output spike is given to the gate of this MOSFET). Therefore, due to the potential difference between two nodes of the memristor, the resistance (or conductance) is decreased (or increased), which exhibits basic spike-timing dependent plasticity in the memristor synapse where the timing difference between presynaptic and postsynaptic spikes results in the differential synaptic weights (differential conductance of the memristor). With a simple memristor model, we show an integrated simulation results by using simulation program with integrated circuit emphasis (SPICE). Furthermore we propose a behavioral model of a unipolar resistive RAM for SPICE, and will demonstrate analog Hopfield neural networks for associative memory using the model (off-line learning). Also we show possible device structures for implementing neural networks having all-to-all synaptic connections.

References

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[2] D.B. Strukov *et al*., Nature, **453**, pp. 80-83, 2008.
[3] G.S. Snider, Nanotechnology, **18**(36), 365202, 2007.