Offset Cancellation with Subthreshold-operated Feedback Circuit for Fully Differential Amplifiers

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***Abstract*—An offset cancellation technique for fully differential amplifiers is proposed. This technique uses subthreshold-operated operational amplifiers (subth-OP amps) for feedback biasing. Two subth-OP amps sense the two outputs of the differential amplifier and accordingly adjust the load currents in the amplifier to fix the outputs to a given reference voltage. The feedback operation is established only at dc and low frequencies because the subth-OP amps operate very slowly. The differential amplifier consequently operates as a high-pass filter and therefore shows no dc offset in its output, while it can normally amplify ac input signals. The results for the simulation and fabrication of the device are described.**

I. INTRODUCTION

Subthreshold circuits are CMOS circuits in which MOSFETs are operated in the subthreshold region, i.e., the region where the gate-source voltage is set smaller than the threshold voltage of MOSFETs [1,2]. Subthreshold circuits operate very slowly because their circuit currents are quite small, on the order of 0.01-10 nA. Making use of their low-speed property can develop new architectures to improve analog-circuit performances. This paper shows one such example, a circuit architecture to cancel the output offset of fully differential amplifiers. The following provides the details on this offset cancellation.

II. OFFSET CANCELLATION WITH A FEEDBACK CIRCUIT OPERATING IN THE SUBTHRESHOLD REGION

Figure 1 conceptually illustrates our idea for offset cancellation. A fully differential amplifier (M_1-M_4 biased by I_{ss}) with a feedback circuit is shown. The feedback circuit consists of two subthreshold-operated operational amplifiers (subth-OP amps) that are explained in the next section.

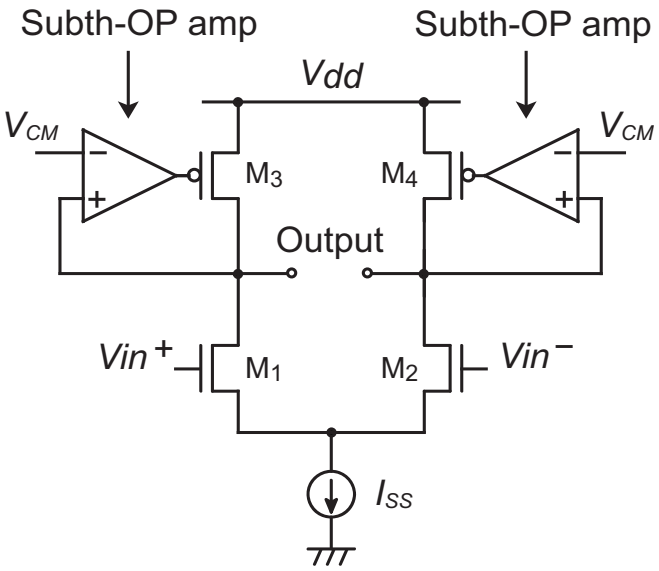


Figure 1. Conceptual topology for offset cancellation.

The subth-OP amps sense the voltages of the two outputs and adjust the gate biases for the load MOSFETs, M_3 and M_4, to fix the outputs to a given common-mode level, V_{CM}. The subth-OP amps operate very slowly with a large time constant (> 1 s), so the feedback is established only at dc and low frequencies. The differential amplifier consequently operates as a high-pass filter and therefore shows no dc offset in its output. ('dc offset' is the sum of an offset due to mismatches in the differential pair M_1-M_4 and an offset due to the dc component of the input signal.) Without the subth-OP feedback circuit, a dc output would be produced and amplified with a high gain to saturate the output of the amplifier. In practice, owing to the feedback through the subth-OP amps, the output offset is set to 0 and the common-mode level is

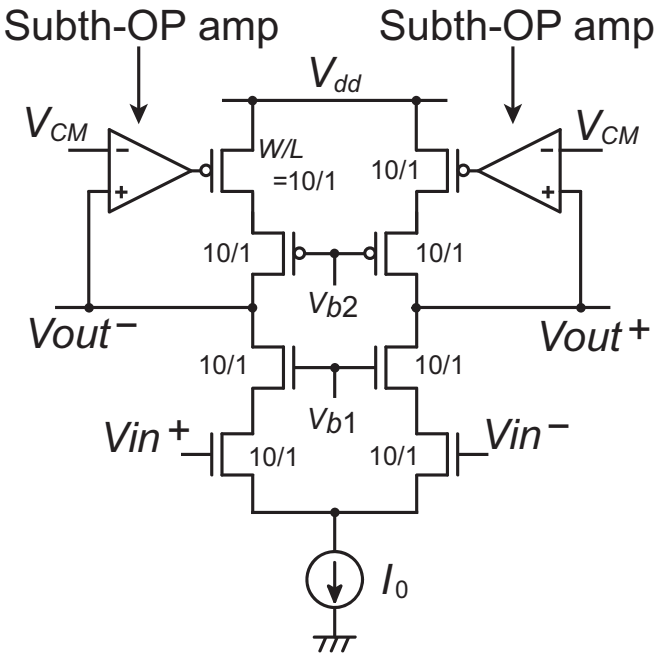


Figure 2. Offset cancellation for cascode differential amplifier. Aspect ratio *W/L* used in device simulation and fabrication is given for each MOSFET.

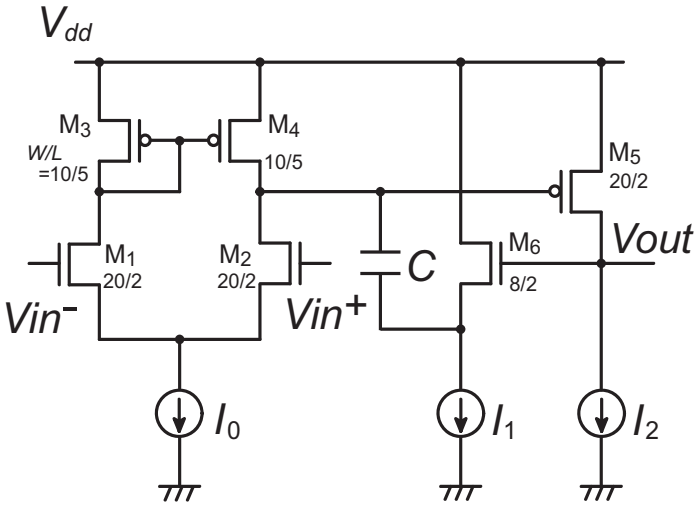


Figure 3. Operational amplifier with input stage operating in the subthreshold region. Aspect ratio *W/L* used in device simulation and fabrication are given for each MOSFET.

fixed to V_{CM} regardless of device properties and mismatches. (Strictly speaking, an offset voltage equal to the input-referred offset voltage of the subth-OP amps appears in the output.) The amplifier has no dc gain but can normally amplify ac input signals. Figure 2 shows the application of this method to a cascode differential amplifier. The results for the simulation and fabrication of this amplifier will be described later.

III. Subthreshold-operated Operational Amplifier

Figure 3 shows the subth-OP amp we used. The circuit topology is the same as that of ordinary two-stage amplifiers [3], but we drove the input stage (M_1-M_4) with very small current I_0 (< 1 nA). Therefore, MOSFETs in the input stage operated in the subthreshold region. The common-source gain stage (M_5) and a source follower (M_6) were driven with ordinary current levels (I_1, I_2 = 10-100 μA).

Figure 4 shows the simulated frequency characteristics of a subth-OP amp. In simulation, we used 0.35-μm CMOS device parameters with MOSFET aspect ratios given in Fig. 3 and a phase compensation capacitance C of 10 pF. The driving currents were set to I_0 = 0.1 nA for the input stage and $I_1 = I_2$ = 10 μA for the gain stage and the source follower. The OP amps operated with a -3dB cutoff frequency of 270 μHz, a unity gain frequency of 32 Hz, and a slew rate of 12 μV/μs.

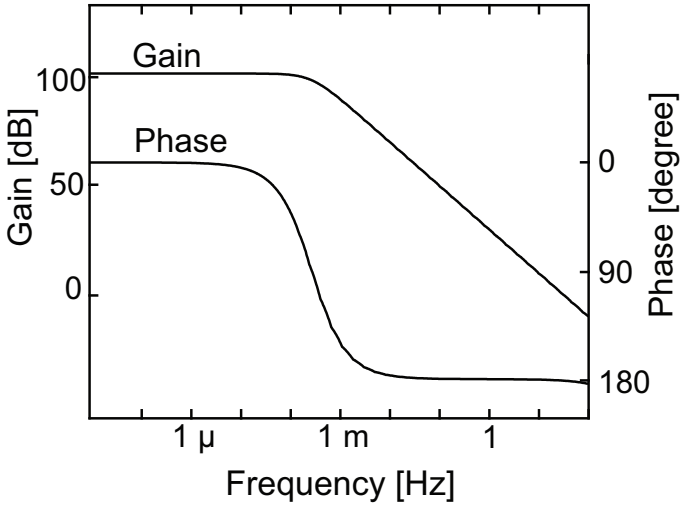


Figure 4. Bode plots for subth-OP amp, simulated using 0.35-μm CMOS device parameters.

IV. Offset Cancellation in Cascode Amplifier: Simulation Results

We confirmed the effect of our offset cancellation for the cascode differential amplifier shown in Fig. 2. We first

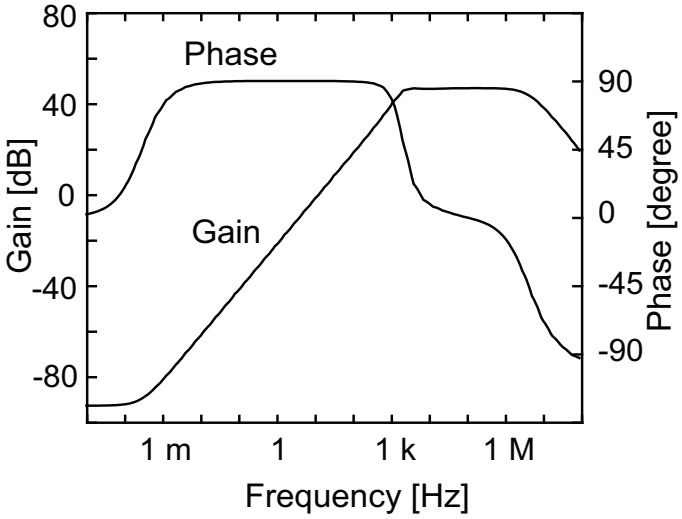


Figure 5. Bode plots for cascode differential amplifier shown in Fig. 2, simulated using 0.35-μm CMOS device parameters.

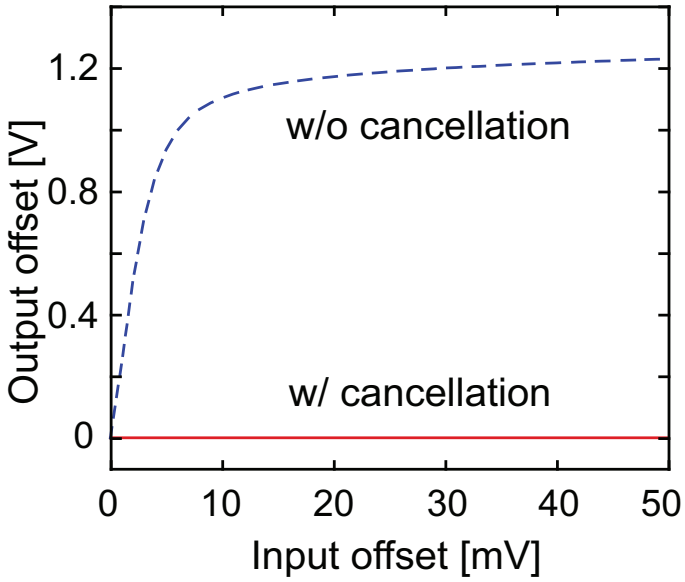
simulated the operation, using a set of 0.35-μm CMOS device parameters, with MOSFET aspect ratios given in Fig. 2 and a tail current I_0 of 200 μA. Parameters used for the subth-OP amps were the same as given in the previous section.

Figure 5 shows the results for bode plots of the amplifier. In this example, the gain was about 47 dB at frequencies from 1 kHz to 10 MHz. For frequencies lower than 1 kHz, the gain decreased as frequency decreased and reached 0 at zero frequency. Owing to the zero dc gain, no dc offset is produced in the output regardless of device properties and mismatches. The circuit can operate as a high gain amplifier at frequencies higher than 1 kHz.

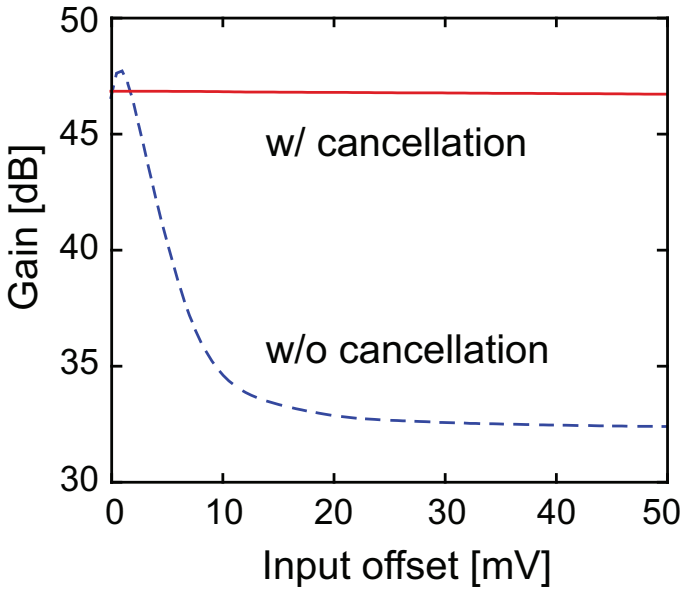
Figure 6 shows the output offset and the gain of the amplifier as a function of an input offset. The solid curves are for the circuit with offset cancellation, and dashed curves without cancellation. An amplifier without offset cancellation has a high dc gain, so its output saturates and gain drops sharply for a small offset, so we cannot use the circuit as an open-loop amplifier. In contrast, with offset cancellation, neither output offset nor gain drop appears, so we can obtain an open-loop amplifier with a high gain.

V. Offset Cancellation in Cascode Amplifier: Measurement Results

We then fabricated a chip implementing this cascode amplifier with offset cancellation, using a 0.35-μm, 2poly-4metal CMOS process. Figure 7(a) shows the micrograph of



(a)



(b)

Figure 6. Effects of offset cancellation in cascode differential amplifier: (a) output offset and (b) gain as a function of input offset, with offset cancellation (solid curves) and without cancellation (dashed curves), simulated for a 100 kHz input signal, using 0.35-μm CMOS device parameters.

the chip (area = 250 μm × 350 μm). Figure 7(b) depicts the measured gain (solid curve) of the amplifier as a function

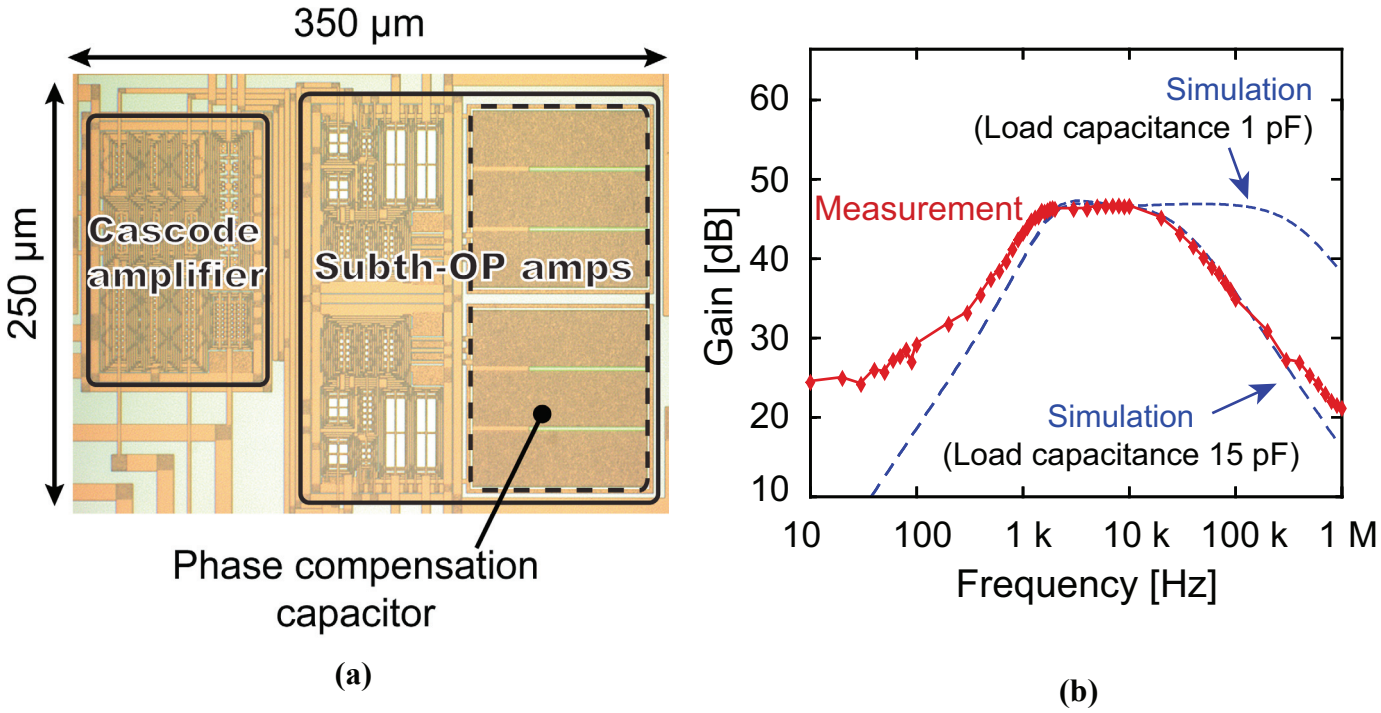


Figure 7. Cascode differential amplifier with subth-OP amps on a chip, fabricated using 0.35-µm, 2poly-4metal CMOS process: (a) chip micrograph (250 µm × 350 µm) and (b) measured gain (solid curve) as a function of frequency, compared with simulation results (dashed curves).

of frequency. The driving conditions were: power supply voltage V_{dd} = 3 V, output common-mode voltage V_{CM} = 1.5 V, and input dc level = 1 V. The dashed curves in the figure show the simulated gain for a load capacitance of 15 pF (the capacitance of the probe used for measurement) and 1 pF.

The -3dB cutoff frequency was 1 kHz. As frequency decreased less than 1 kHz, the gain also decreased. The decrease was, however, smaller than expected. We are analyzing the factors leading this problem. The measured dc gain was 0, so the circuit can be used as an offset-canceled, high-gain amplifier.

VI. Conclusion

We proposed a method of canceling the offset of differential amplifiers with a feedback circuit consisting of subth-OP amps. The feedback operation is established at dc and low frequencies because the subth-op amps operate very slowly. This removes the offset of the differential amplifier. For ac input signals, the amplifier operates normally with a high gain.

Acknowledgment

This work is supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc.

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