Low Voltage Operation of Master-Slave Flip-Flops for Ultra-Low Power Subthreshold LSIs

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Abstract

In this paper, we investigate low voltage operation of master-slave flip-flops (MSFFs) for ultra-low power subthreshold CMOS LSI families. Static MSFF, which consists of NAND gates, shows the most stable operation, while dynamic MSFFs are unsuitable for low voltage operation because switching gates fail to operate at low voltage. Low voltage limitation of static MSFF depends on that of CMOS gates. We also reveal and confirm theoretically that threshold voltage difference between nMOS and pMOS transistors affect output characteristics of CMOS logic gates significantly in subthreshold operation.

Keywords: subthreshold, flip-flop, low-power, low-voltage, inverter

1. Introduction

New social information infrastructures, or ”ubiquitous” network systems, will be developed to provide promising communication platforms for collecting and delivering information throughout the world. Such systems will need a huge number of distributed smart sensor LSIs to measure various physical data in our surroundings, store and process the measured data, and output the data on demand (see [1], [2] for an example of such sensors). These sensing LSIs must operate with ultra-low power, e.g., a few microwatts or less, because they will probably be placed under conditions where they have to get their necessary energy from microbatteries or from less-than-ideal surroundings such as ones with poor sunlight, weak electric waves, and slight differences in daytime and nighttime temperatures.

Figure 1 depicts the architecture of such smart sensor LSIs. The LSI consists of sensors, AD/DA converters, digital signal processors, memories, reference circuits, and power supply circuits. To achieve microwatt operation, all of the circuits in the LSI have to be operated in the subthreshold region of MOSFETs, i.e., a region at which the gate-source voltage of MOSFETs is lower than the threshold voltage. In general, CMOS digital gates consume low power dissipation. However, for such a power-aware LSI application, CMOS digital gates also have to be operated under a low power supply voltage to further reduce the power dissipation.

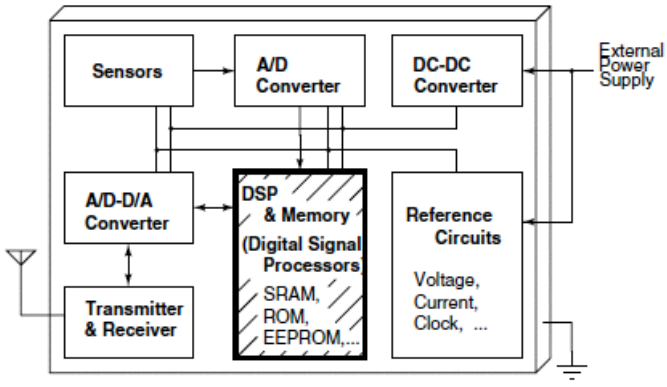

Fig.1. Chip architecture for microwatt power-aware smart-sensor LSIs.

Sequential circuits designed with flip-flops or latches are one of the most important logic circuit in LSIs to perform various digital signal processing. Master-slave flip-flop (MSFF) is such one that is widely used as a temporal memory. A comparative study on the performance of MSFFs for low voltage operation has been reported in [3]. However, the discussion on low power operation of MSFFs was quite limited on nominal supply voltage and the most suitable architecture for

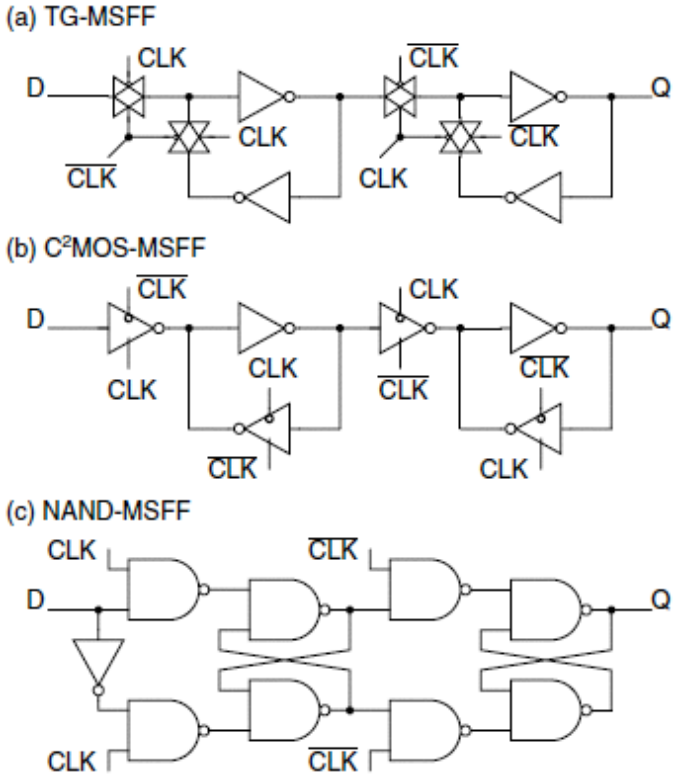

Fig. 2. Three different flip-flop architectures. Dynamic MSFFs: (a)TG-MSFF and (b)C^{2}MOS-MSFF, and a static MSFF: (c)NAND-MSFF.

subthreshold operation was not clear. Therefore, we need to analyze the performance of MSFFs in subthreshold operation in more detail.

In this paper, we investigate low voltage operation of MSFFs in detail and propose the most suitable architecture of MSFFs for subthreshold digital circuit designs. This paper is organized as follows: low voltage operations of MSFFs with different architectures are investigated in Sect. 2, low voltage operation of CMOS gates in MSFFs are discussed in Sect. 3, and we conclude the paper in Sect. 4.

2. Low Power Operation of MSFFs

Figure 2 shows three widely used MSFF circuit designs – two dynamic MSFFs: (a) four transmission gates and four inverters (TG-MSFF) and (b) four clocked-CMOS inverters and two CMOS inverters (C^{2}MOS-MSFF), and a static MSFF: (c) eight NAND gates and an inverter (NAND-MSFF). The MSFFs can be configured as a toggle flip-flop (TFF) circuit. With this configuration, clock-to-Q delay of each circuit was investigated by changing power supply voltage V_{DD}.

We analyzed the operation of the circuits by a

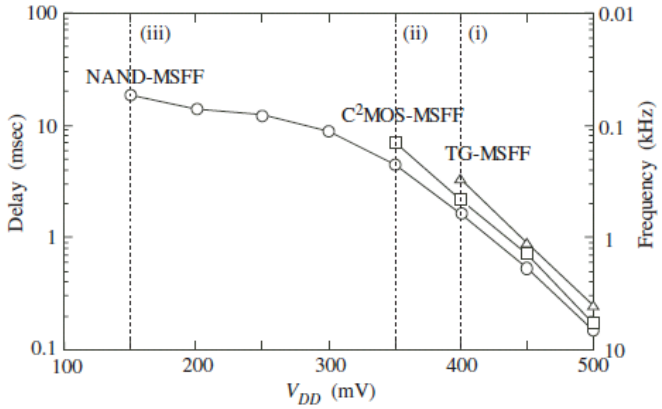

Fig. 3. Simulated clock-to-Q delay time and corresponding frequency of MSFFs as a function of power supply voltage V_{DD}.

SPICE simulation with a set of 0.35-μm 2P4M standard CMOS parameters. Typical threshold voltages of nMOS and pMOS transistors we used are 0.50 V and 0.65 V, respectively. Because we focused on low voltage operation of MSFFs, ratioed-designs were not considered in this work. Therefore, all of the nMOS and pMOS transistors were set to minimum feature size of W/L = 0.4 μm / 0.35 μm.

Figure 3 shows the simulated clock-to-Q delay time and corresponding frequency as a function of power supply voltage V_{DD}. TG-MSFF and C^{2}MOSMSFF could not operate correctly at 400 mV and 350 mV, respectively. NAND-MSFF operated at the lowest supply voltage of 150 mV. These results show that static MSFF is suitable and dynamic MSFFs are unsuitable for low voltage operation. This is because dynamic MSFFs have disadvantage in that the circuits consist of switching gates – transmission gates and clocked CMOS gates.

In TG-MSFF, transmission gates could not operate correctly at low voltage. This is because on-resistance of the transmission gate increases with decreasing power supply voltage. Moreover, because transmission gates are used to open or shunt the signal path, source/drain terminals are connected to floating node of the circuit. Therefore, transmission gates could not be applied sufficient gate-source voltage V_{GS}. This also increases on-resistance of the transmission gate. Therefore, transmission gate fails its operation and TG-MSFF could not operate correctly.

In C^{2}MOS-MSFF, clocked CMOS inverters are used instead of transmission gates. Unlike TG-MSFF, clocked CMOS inverters have switching function internally. Larger gate-source voltage for switch transistor can be obtained easily compared to transmission gates. Therefore, C^{2}MOS-MSFF can operate lower supply voltage than TG-MSFF. However, when the

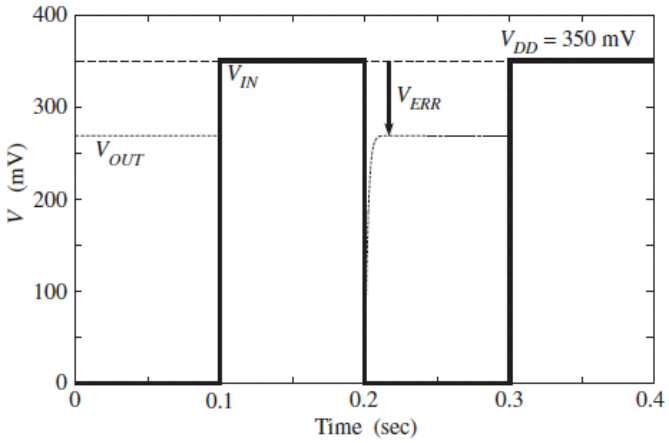

Fig. 4. Transient response of CMOS NOT gate (inverter) at a low power supply voltage of 350 mV. CMOS inverter cannot achieve a full-swing operation at input voltage of 0 V.

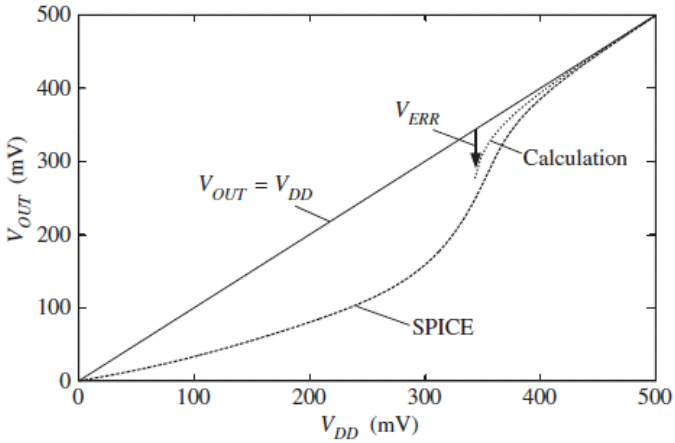

Fig. 5. Simulated output voltage of an inverter when input voltage is 0 V, as a function of power supply voltage V_{DD}. Ideal output voltage and calculated voltage using Eq. (5) are also plotted.

power supply voltage is decreased to about 350 mV, clocked CMOS inverters also lose its switching function and then C^2MOS-MSFF fails its operation.

NAND-MSFF consists of eight NAND gates and an inverter as shown in Fig. 2 (c) without using any transmission gates and clocked CMOS gates. Therefore, low voltage limitation of the circuit depends on that of CMOS logic gates. Because CMOS logic gates can operate lower voltage than switching gates, NAND-MSFF shows the most stable operation at the expense of the transistor number increase. In the next section, low power limitation of CMOS gates is discussed in more detail.

3. Low Power Operation of the CMOS Gates

NAND-MSFF can operate at the lowest power supply voltage as shown in Fig. 3. The low voltage limitation of NAND-MSFF depends on that of CMOS gates. Figure 4 shows the simulated transient response of CMOS inverters at power supply voltage of 350 mV. CMOS inverter could not achieve a full swing output when input voltage was 0 V. The decrease in output voltage, or error voltage V_{ERR}, comes from threshold voltage difference between nMOS and pMOS transistors. As mentioned above, in the CMOS process we used, threshold voltage of pMOS transistor is larger than that of nMOS transistor ($V_{TH,p}$ = 0.65 V > $V_{TH,n}$ = 0.5 V). Therefore, the driving current of pMOS transistor is significantly smaller than that of nMOS transistor with the same gate-source voltage. As power supply voltage decreases, there is a voltage that pMOS on-currents are comparable with nMOS off-currents even if gate-source voltage of pMOS transistor equals to power supply voltage V_{DD}. Therefore, output voltage of inverter begins to decrease from power supply voltage V_{DD}. This can be confirmed as follows.

The subthreshold drain current, I_D, through a MOSFET is an exponential function of gate-source voltage V_{GS} and drain source voltage V_{DS}, and is given by

$$I_D = I_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right)\left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right) \quad (1)$$

$$I_0 = K\mu C_{OX} V_T^2 (\eta - 1) \quad (2)$$

where K is the aspect ratio of the MOSFET, μ is the mobility, C_{OX} is the gate-oxide capacitance, V_T (= k_BT/q) is the thermal voltage, η is the subthreshold slope factor, and V_{TH} is the threshold voltage of the MOSFET [4], [5]. For a drain-source voltage V_{DS} higher than 0.1 V, drain voltage dependence of the current can be ignored and the current is rewritten as

$$I_D = I_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) \quad (3)$$

Around the power supply voltage where error voltage V_{ERR} begins to increase, V_{ERR} can be analyzed theoretically. V_{ERR} can be given by

$$V_{ERR} = V_{DD} - V_{OUT} \quad (4)$$

where V_{OUT} is the output voltage of inverter when the input voltage is 0 V. At this condition, pMOS transistor

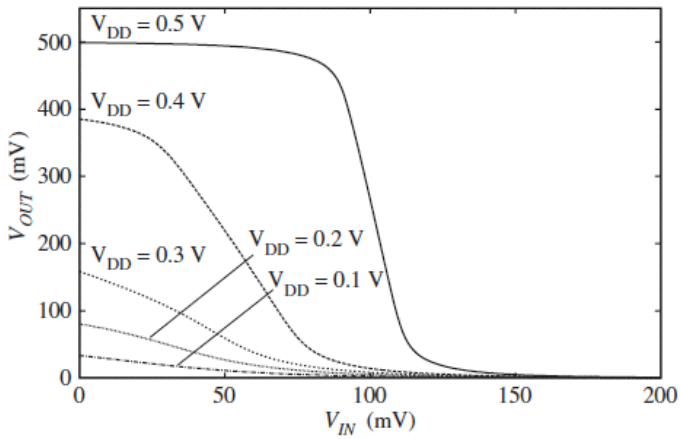

Fig. 6. Transfer characteristics of an inverter with power supply voltage as a parameter.

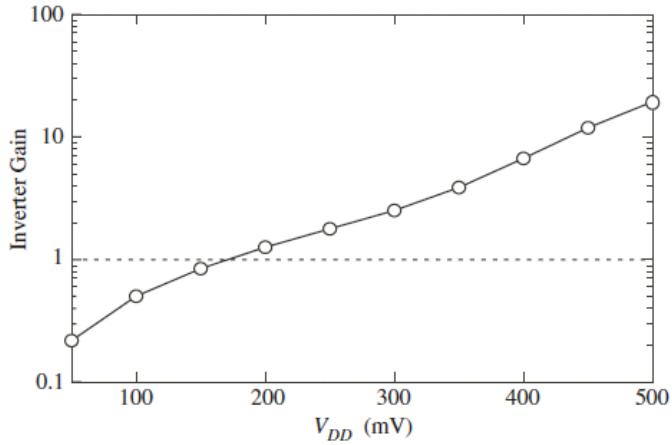

Fig. 7. Voltage gain of an inverter as a function of power supply voltage V_{DD}. Voltage gain decreases with decreasing power supply voltage and becomes 1 or less at power supply voltage of 170 mV.

operates in the subthreshold and linear region, while nMOS transistor operates in the subthreshold and saturate region. Therefore, current characteristics of pMOS and nMOS transistors are expressed by Eqs. (1) and (3), respectively. From Eqs. (1), (3), and (4), V_{ERR} can be derived and is expressed as

$$V_{ERR} = -V_T \ln\left(1 - \frac{I_{o,n}}{I_{o,p}} \exp\left(\frac{\left(V_{TH,p} - V_{TH,n}\right) - V_{DD}}{\eta V_T}\right)\right) \quad (5)$$

Because both threshold voltage difference $V_{TH,p}$ - $V_{TH,n}$ and power supply voltage V_{DD} are contained in the exponential function, larger threshold voltage difference induces error voltage V_{ERR} on the output when

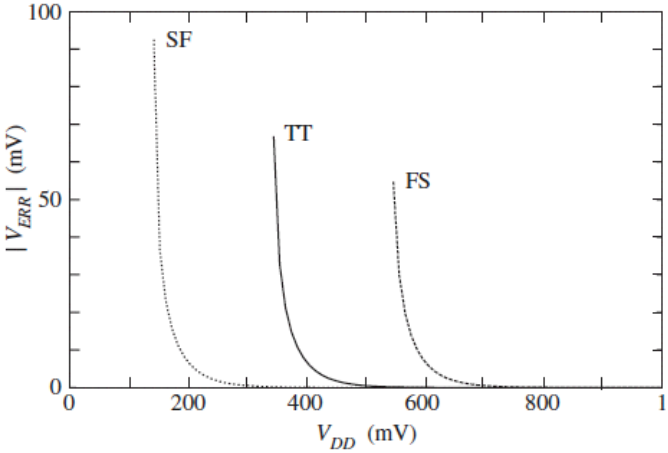

Fig. 8. Simulated V_{ERR} from corner analysis. Process corners of nMOS and pMOS devices, such as Slow (S), Typical (T), and Fast (F), were considered in the simulation.

power supply voltage V_{DD} becomes low. Note that if threshold voltage of nMOS transistor is larger than that of pMOS transistor, error voltage V_{ERR} appears around ground level when input voltage is V_{DD}.

Figure 5 shows the simulated output voltage V_{OUT} of the inverter when input voltage is 0 V, as a function of power supply voltage. Ideal output voltage, $V_{OUT} = V_{DD}$, and calculated output voltage by using Eq. (5), or $V_{OUT} = V_{DD} - V_{ERR}$, were also plotted in the figure. The simulated and calculated output voltage decreased at almost same voltage about 450 mV. By using Eq. (5), we can predict power supply voltage where output voltage begins to decrease.

Figure 6 shows the transfer characteristics of the inverter at different power supply voltages. At higher power supply voltages, inverter operates correctly. However, as the power supply voltage decreases, V_{ERR} increases and the inverter gain decreases significantly. Figure 7 shows inverter voltage gain (V_{OUT}/V_{IN}) in log-scale as a function of power supply voltage. Inverter voltage gain deceases with decreasing power supply voltage and becomes 1 or less at 170 mV. This result indicates that inverter cannot perform logic operation below 170 mV. This result corresponds with the low power limitation of NAND-MSFF as shown in Fig. 3.

To verify the stability of the circuit operation, process corner analysis was performed by using parameters provided by the manufacturer. Process corners of nMOS and pMOS devices such as Slow (S), Typical (T), and Fast (F) were considered in the simulation. Figure 8 shows simulated results of error voltage V_{ERR}. In the figure, “SF” means that nMOS transistors are in slow condition and pMOS transistors are in fast condition. At “SF” corner, V_{ERR} increases at lower power supply voltage of 300 mV. Meanwhile, at “FS” corner, V_{ERR}

increases at higher power voltage of 700mV. By using Eq. (5), these results can be understood as follows. At "SF" condition, threshold voltages of nMOS and pMOS transistors are higher and lower than typical value, respectively, the threshold voltage difference between nMOS and pMOS transistors becomes small and then the error voltage V_{ERR} appears at lower voltage. In a similar way, at "FS" condition, threshold voltages of nMOS and pMOS transistors are lower and higher, respectively, the threshold voltage difference becomes large and then the error voltage V_{ERR} appears at higher voltage. By using Eq. (5), we can predict the characteristic of error voltage V_{ERR} in CMOS gates.

From these analyses, CMOS logic gate operated in subthreshold region changes its logic function drastically with process corner variation. Therefore, compensation techniques are required for stable operation. As discussed above, variation of threshold voltage is one of the most critical problems in subthreshold LSI designs. Therefore, we are now developing an on-chip power management circuit system that can change power supply voltage by using a voltage reference circuit in [7] for stable operation.

4. Conclusion

In this paper, we investigated low voltage operation of MSFFs for ultra-low power subthreshold MOS LSIs, by using 0.35-μm standard CMOS process parameters. Static MSFF—NAND-MSFF— shows the most stable operation and is suitable for low power supply voltage operation. Dynamic MSFFs —TG-MSFF and C^2MOS-MSFF— are unsuitable for low voltage operation because switching gates fail to operate at low power supply voltage. Low voltage limitation of static MSFF depends on that of CMOS gates. We also reveal and confirm theoretically that threshold voltage difference between nMOS and pMOS transistor affects output characteristics significantly in subthreshold operation.

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