Analog CMOS Circuits Implementing Neural Segmentation Model Based on Symmetric STDP Learning

Gessyca Maria Tovar[1], Eric Shun Fukuda[2], Tetsuya Asai[1], Tetsuya Hirose[1], and Yoshihito Amemiya[1]

[1] Hokkaido University, Kita 14, Nishi 9, Kita-ku, Sapporo, 060-0814 Japan
gessyca@sapiens-ei.eng.hokudai.ac.jp,
http://sapiens-ei.eng.hokudai.ac.jp/
[2] Tokyo University, Kashiwanoha 5-1-5, Kashiwa-shi, Chiba 277-8561, Japan

Abstract. We proposed a neural segmentation model that is suitable for implementation in analog VLSIs using conventional CMOS technology. The model consists of neural oscillators mutually couple through synaptic connections. The model performs segmentation in temporal domain, which is equivalent to segmentation according to the spike timing difference of each neuron. Thus, the learning is governed by symmetric spike-timing dependent plasticity (STDP). We numerically demonstrate basic operations of the proposed model as well as fundamental circuit operations using a simulation program with integrated circuit emphasis (SPICE).

1 Introduction

The human brain has the ability to group elements from multiple sensory sources. Synchronous activity has been observed in many parts of the brain, e.g., in the visual and auditory cortex. These discoveries have triggered much interest in exploring oscillatory correlation to solve the problems of neural segmentation. Many neural models that perform segmentation have been proposed, e.g., [1,2,3], but they are often difficult to implement on practical integrated circuits. A neural segmentation model called LEGION (Locally Excitatory Globally Inhibitory Oscillator Networks) [4], can be implemented on LSI circuits [5]. However, the LEGION model fails to work in the presence of noise. Our model solves this problem by including spike-timing dependent plasticity (STDP) learning with all-to-all connections of neurons.

In this paper, we present a simple neural segmentation model that is suitable for analog CMOS circuits. The segmentation model is suitable for applications such as figure-ground segmentation and the cocktail-party effect, etc.

The model consists of mutually coupled (all-to-all) neural oscillators that exhibit synchronous (or asynchronous) oscillations. All the neurons are coupled with each other through positive or negative synaptic connections. Each neuron accepts external inputs, e.g., sound inputs in the frequency domain, and oscillates (or does not oscillate) when the input amplitude is higher (or lower) than a

M. Ishikawa et al. (Eds.): ICONIP 2007, Part II, LNCS 4985, pp. 117–126, 2008.

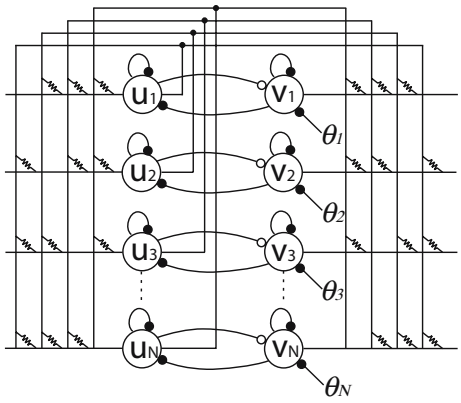

Fig. 1. Network construction of segmentation model

given threshold value. The basic idea is to strengthen (or weaken) the synaptic weights between synchronous (or asynchronous) neurons, which may result in phase-domain segmentation. The synaptic weights are updated based on symmetric STDP using Reichardt's correlation neural network [6] which is suitable for analog CMOS implementation.

2 The Model and Basic Operations

Our segmentation model is illustrated in Fig. 1. The network has N neural oscillators consisting of the Wilson-Cowan type activator and inhibitor pairs (u_i and v_i) [7]. All the oscillators are coupled with each other through resistive synaptic connections, as illustrated in the figure. The dynamics are defined by

$$\tau \frac{du_i}{dt} = -u_i + f_{\beta_1}(u_i - v_i) + \sum_{j \neq i}^{N} W_{ij}^{\mathrm{uu}} u_j, \tag{1}$$

$$\frac{dv_i}{dt} = -v_i + f_{\beta_2}(u_i - \theta_i) + \sum_{j \neq i}^{N} W_{ij}^{\mathrm{uv}} u_j, \tag{2}$$

where τ represents the time constant, N the number of oscillators, θ_i the external input to the i-th oscillator. $f_{\beta_i}(x)$ represents the sigmoid function defined by $f_{\beta_i}(x) = [1 + \tanh(\beta_i x)]/2$, W_{ij}^{uu} the connection strength between the i-th and j-th activators and W_{ij}^{uv} the strength between the i-th activator, and the j-th inhibitor. The operation of the model and the simulations of nullclines and trajectory are explained in [8].

According to the stability analysis in [7], the i-th oscillator exhibits excitable behaviors when $\theta_i < \Theta$ where $\tau \ll 1$ and $\beta_1 = \beta_2$ ($\equiv \beta$), where Θ is given by

$$\Theta = u_0 - \frac{2}{\beta} \tanh^{-1}(2v_0 - 1), \tag{3}$$

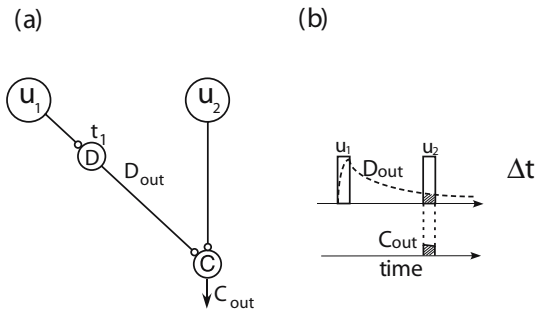

Fig. 2. Reichardt's correlation network

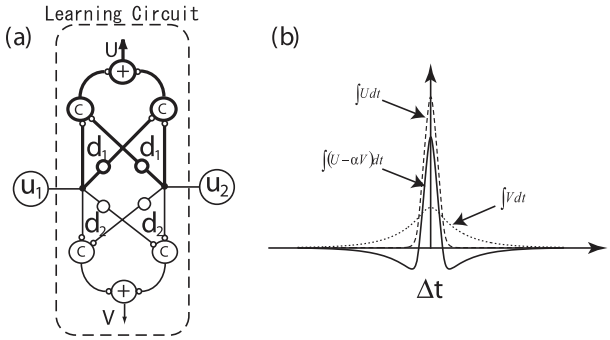

Fig. 3. Learning characteristic: Reichardt's correlation

$$u_0 \equiv \frac{1-\sqrt{1-4/\beta}}{2},$$
$$v_0 \equiv u_0 - \frac{2}{\beta}\tanh^{-1}(2u_0 - 1),$$

and exhibits oscillatory behaviors when $\theta_i \geq \Theta$, if W_{ij}^{uu} and W_{ij}^{uv} for all i and j are zero.

Suppose that neurons are oscillating ($\theta_i \geq \Theta$ for all i) with different initial phases. The easiest way to segment these neurons is to connect the activators belonging to the same (or different) group with positive (or negative) synaptic weights. In practical hardware, however, the corresponding neuron devices have to be connected by special devices having both positive and negative resistive properties, which prevents us from designing practical analog circuits. Therefore, we simply use positive synaptic weights between activators and inhibitors, and do not use negative weights. When the weight between the i-th and j-th activators (W_{ij}^{uu}) is positive and W_{ij}^{uv} is zero, the i-th and j-th activators will be synchronized. Contrarily, when the weight between the i-th activator and the j-th inhibitor (W_{ij}^{uv}) is positive and W_{ij}^{uu} is zero, the i-th and j-th activators

will exhibit asynchronous oscillation because the j-th inhibitor (synchronous to the i-th activator) inhibits the j-th activator.

The synaptic weights (W_{ij}^{uu} and W_{ij}^{uv}) are updated based on our assumption; one neural segment is represented by synchronous neurons, and is asynchronous with respect to neurons in the other segment. In other words, neurons should be correlated (or anti-correlated) if they received synchronous (or asynchronous) inputs. These correlation values can easily be calculated by using Reichardt's correlation neural network [6] which is suitable for analog circuit implementation [9]. The basic unit is illustrated in Fig. 2(a). It consists of a delay neuron (D) and a correlator (C). A delay neuron produces blurred (delayed) output D_{out} from spikes produced by activator u_1. The dynamics are given by

$$d_1 \frac{dD_{\mathrm{out}}}{dt} = -D_{\mathrm{out}} + u_1, \tag{4}$$

where d_1 represents the time constant. The correlator accepts D_{out} and spikes produced by activator u_2 and outputs $C_{\mathrm{out}} = D_{\mathrm{out}} \times u_2$. The conceptual operation is illustrated in Fig. 2(b). Note that C_{out} qualitatively represents correlation values between activators u_1 and u_2 because C_{out} is decreased (or increased) when Δt, inter-spike intervals of the activators, is increased (or decreased). Since this basic unit can calculate correlation values only for positive Δt, we use two basic units, which we call a unit pair, as shown by thick lines in Fig. 3(a). The output (U) is thus obtained for both positive and negative Δt by summing the two C_{out}s. Through temporal integration of U, we obtain impulse responses of this unit pair. The sharpness is increases as $d_1 \to 0$. Introducing two unit pairs with different time constants, i.e., d_1 and d_2 ($\gg d_1$), one can obtain those two impulse responses (U and V) simultaneously. The impulse responses (U and V) are plotted in Fig. 3(b) by a dashed and a dotted line, respectively. The weighted subtraction ($U - \alpha V$) produces well-known Mexican hat characteristics, as shown in Fig. 3(b) by a solid line. We use this symmetric characteristic for the weight updating as a spike-timing dependent plasticity (STDP) in the oscillator network.

Our learning model is shown in Fig. 4(a). The learning circuit is located between two activators u_1 and u_2. The two outputs (U and V) of the learning circuit are given to interneuron W which performs subtraction $U - \alpha V$. According to our above assumptions for neural segmentation, when $U - \alpha V$ is positive, the weight between activators u_1 and u_2 (illustrated by a horizontal resistor symbol in Fig. 4(a)) is increased because the activators should be correlated. On the other hand, when $U - \alpha V$ is negative, the weight between activator u_1 and inhibitor v_2 (illustrated by a slant resistor symbol in Fig. 4(a)) is increased because activators u_1 and u_2 should be anti-correlated. To this end, the output of interneuron W is given to two additional interneurons (f_{uu} and f_{uv}). The input-output characteristics of these interneurons are shown in Figs. 4(b). Namely, f_{uu} (or f_{uv}) increases linearly when positive (or negative) $U - \alpha V$ increases, but is zero when $U - \alpha V$ is negative (or positive). Those positive outputs (f_{uu} and f_{uv}) are given to the weight circuit to modify the positive resistances. The dynamics

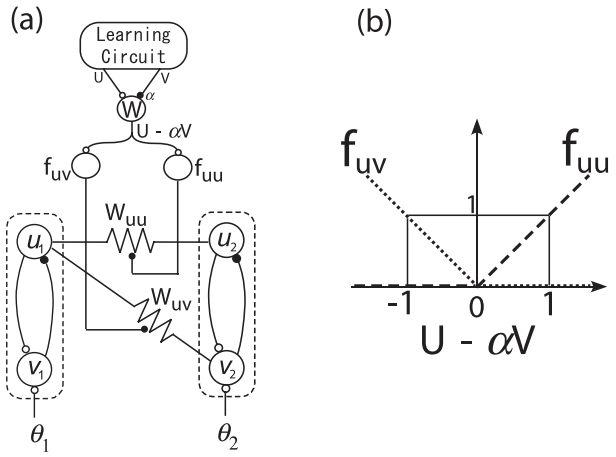

Fig. 4. STDP learning Model

of the "positive" weight between activators u_i and u_j is given by

$$\frac{dW_{ij}^{\mathrm{uu}}}{dt} = -W_{ij}^{\mathrm{uu}} + f_{\mathrm{uu}}, \tag{5}$$

and the "positive" weight between activator u_i and inhibitor v_j is

$$\frac{dW_{ij}^{\mathrm{uv}}}{dt} = -W_{ij}^{\mathrm{uv}} + f_{\mathrm{uv}}. \tag{6}$$

We carried out numerical simulations with $N = 6$, $\tau = 0.1$, $\beta_1 = 5$, $\beta_2 = 10$, $d_1 = 2$, $d_2 = 0.1$ and $\alpha = 1.2$. Time courses of activators u_i ($i = 1 \sim 6$) are shown in Fig. 5. Initially, the external inputs θ_i ($i = 1 \sim 6$) were zero ($< \Theta$), but θ_i for $i = 1 \sim 3$ and $i = 4 \sim 6$ were increased to 0.5 ($> \Theta$) at $t = 10$ s and 20.9 s, respectively. We observed that $u_{1\sim3}$ and $u_{4\sim6}$ were gradually desynchronized without breaking synchronization amongst neurons in the same group, which indicated that segmentation of neurons based on the input timing was successfully achieved.

3 CMOS Unit Circuits and Operations

The construction of a single neural oscillator is illustrated in Fig. 6. The oscillator consists of two differential pairs (m_3-m_4 and m_8-m_9), two current mirrors (m_1-m_2 and m_6-m_7), bias transistors (m_5 and m_10); and two additional capacitors (C_1 and C_2). To explain the basic operation of the neural oscillator, let us suppose that W_{uu} and W_{uv} in Eqs. (1) and (2) are zero. Now in Eq. (1), when u is larger than v ($u > v$) u tends to increase and approach to 1 (vdd), on the contrary, when u is lower than v ($u < v$) u tends to decrease and approach to

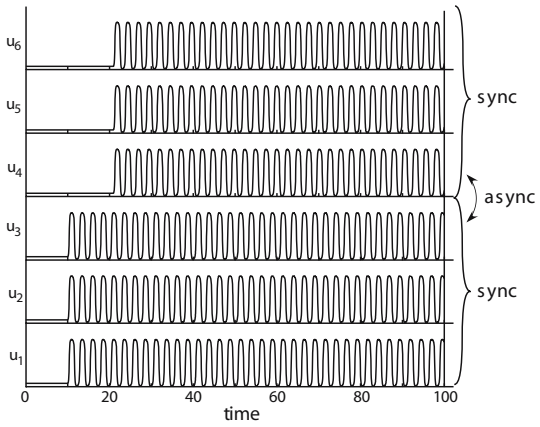

Fig. 5. Numerical simulation results

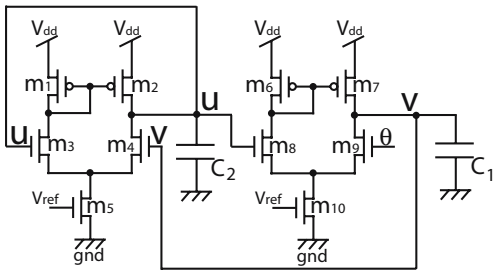

Fig. 6. Unit circuits for neural segmentation

0 (gnd). The same analysis can be apply to Eq. (2). When u is larger than θ ($u > \theta$) v tends to increase approaching to (vdd), and, when u is lower than θ ($u < \theta$) v tends to decrease and approaching to (gnd).

The nullclines (steady state voltage) of a single neuron circuit were simulated in [8]. Transient simulation results of the neuron circuit are shown in Fig. 7. The parameter used for the transistors were obtained from MOSIS AMIS 1.5-μm CMOS process. All transistor sizes were fixed at $L = 1.6$ μm and $W = 4$ μm, the capacitors (C_1 and C_2) were set at 0.1 pF, and the differential amplifier's V_{ref} was set at 0.7 V, and the supply voltage was set at 5 V. Time courses of the activator unit (u) and (v) are shown. Initially, θ was set at 0.5 V (in relaxing state), and neither u nor v oscillated, instead u they are in equilibrium. Then θ was increased to 2.5 V at $t = 5$ μs, and both u and v exhibited oscillations with small phase difference between them. Again, θ was set at 0.5 V at $t = 10$ μs and u relaxed, and v to a high value (around V_{dd}) and decreases with time until it reach equilibrium, as expected.

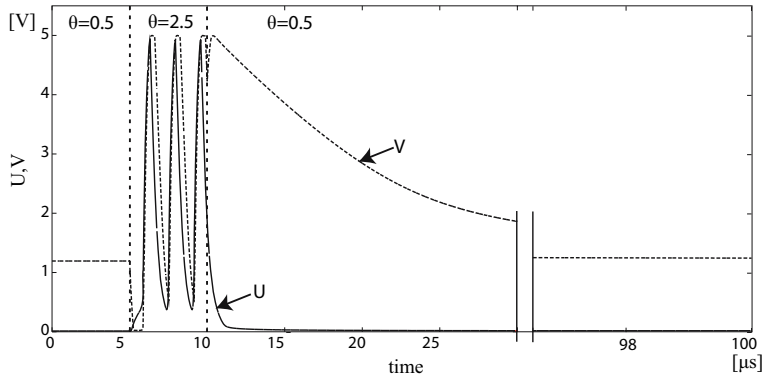

Fig. 7. Simulation results of neural oscillator

A circuit implementing Reichardt's basic unit shown in Fig. 2(a) is shown in Fig. 8. Bias current I_1 drives m_6. Transistor m_5 is thus biased to generate I_1 because m_5 and m_6 share the gates. When m_3 is turned on (or off) by applying V_{dd} (or 0) to u_1, I_1 is (or is not) copied to m_1. Transistors m_1 and m_2 form a current mirror, whereas m_2 and m_4 form a pMOS source-common amplifier whose gain is increased as $V_{b1} \to 0$. Since the parasitic capacitance between the source and drain of m_2 is significantly amplified by this amplifier, temporal changes of u_1 are blurred on the amplifier's output (D_{out}). Therefore this "delayer" acts as a delay neuron in Fig. 2(a). A correlator circuit consists of three differential amplifiers (m_{12}-m_{13}, m_{14}-m_{15} and m_{16}-m_{17}), a pMOS current mirror (m_{19}-m_{20}), a bias transistor (m_{18}) and a bias current source (I_2). In this circuit, m_{12}, m_{14} and m_{17} are floating gate transistors. They reduce voltages of D_{out} and u_2 to $D_{out}/10$ and $u_2/10$ because the input gate sizes were designed to 'capacitively' split the input voltages with the ratio of 1:10. The output current of differential pair m_{14}-m_{15} is:

$$I_{out} = I_2 f(D_{out}/10) f(u_2/10), \tag{7}$$

where $f(x)$ is the sigmoid function given by $f(x) = 1/(1 + e^{-x})$. Current I_{out} is regulated by the bias transistor m_{18}. The result is copied to m_{20} through current mirror m_{19}-m_{20}. This operation corresponds to that of a correlator in Fig. 2(a).

We carried out circuit simulations of the above circuits. The parameter sets we used for the transistors were obtained from MOSIS AMIS 1.5-μm CMOS process. Transistor sizes of all nMOS and pMOS m_9, m_{10} and m_{18} were fixed at $L = 1.6$ μm and $W = 4$ μm pMOS transistors m_1, m_2, m_{19} and m_{20} were fixed at $L = 16$ μm and $W = 4$ μm. The supply voltage was set at 5 V.

Simulation results of our STDP circuits are shown in Fig. 9. Parameters V_{b1}, V_{b2} and V_{b3} were set at 0.41 V, 0.7 V and 4.1 V, respectively. The value of V_{b1} was chosen so that the delayer makes a reasonable delay. Horizontal axes (Δt) in Fig. 9 represent time intervals of input current pulses (spikes). Voltage

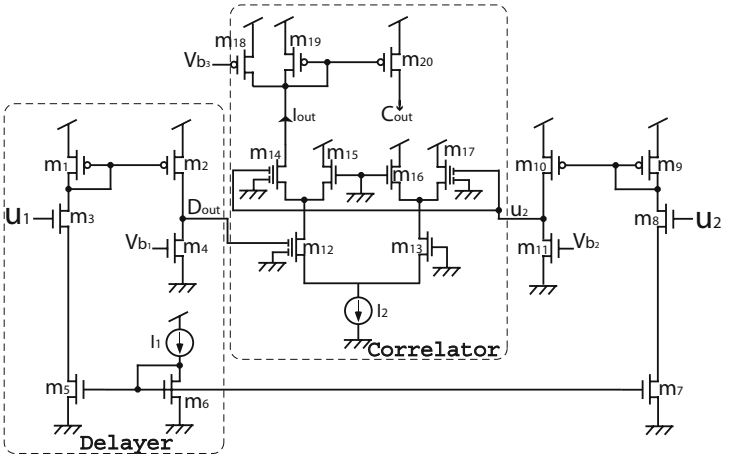

Fig. 8. STDP circuit

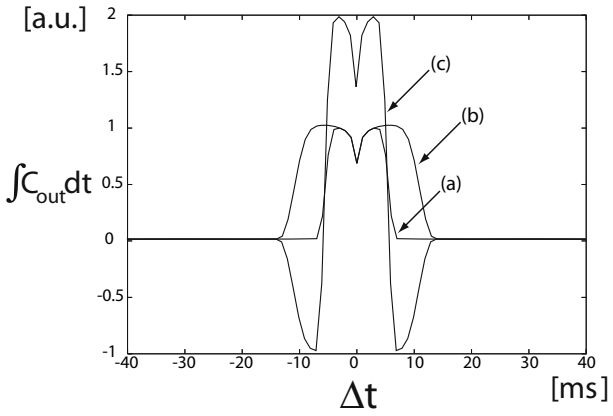

Fig. 9. STDP characteristics

pulses (amplitude: 5 V, pulse width: 10 ms) were applied as u_1 and u_2 in Fig. 8. We integrated C_{out} during the simulation and plotted normalized values [(a) in Fig. 9]. Then we changed the value of V_{b_1} to 0.37 V. The lowered V_{b1} reduced the drain current of m_4 and made the delay larger. Again, C_{out} was integrated and normalized. The result is plotted [(b) in Fig. 9]. By subtracting (b) from tripled (a), we obtained the STDP learning characteristic (c) in Fig. 9.

Simulations for testing the synaptic weights of two coupled neural oscillators were made. Figure 10(a) shows the two oscillators with all the synaptic connections. The oscillation of neurons u_1 and u_2 without applying any connection between them (V_{gs}=0 V for W_{uu} and W_{uv}) are shown in Fig. 10(b) where the neurons oscillated independently. nMOS transistors with $L = 1.6$ μm and $W = 4$

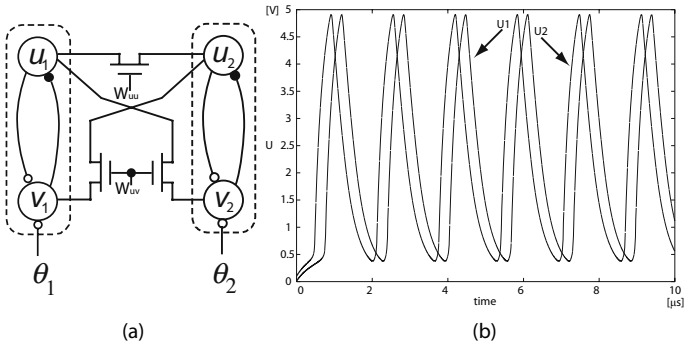

Fig. 10. (a) Coupled neural oscillators (b) u_1 and u_2 oscillations

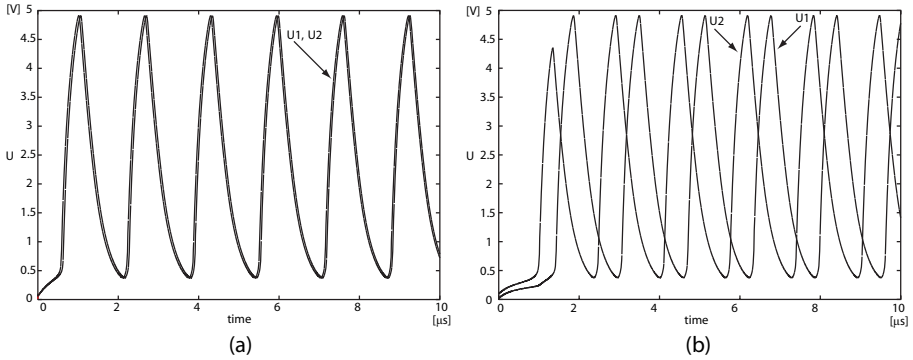

Fig. 11. Oscillation of neurons u_1 and u_2 when (a)excitation is applied and (b) inhibition is applied

μm were used as synaptic weight W_{uu} and W_{uv}, Fig. 10(a) shows the excitatory connection W_{uu} between neurons u_1 and u_2, and inhibitory connections W_{uv} between neurons $u_{1,2}$ and $v_{2,1}$. The oscillations of neurons u_1 and u_2 when applying an excitation through W_{uu} (the gate voltage of W_{uu} was set at 1 V and 0 V for W_{uv}) are shown in Fig. 11(a), in this case both neurons synchronized. On the contrary, when applying an inhibition through W_{uv} (the gate voltage of W_{uv} was set at 0.6 V and 0 V for W_{uu}) the neurons oscillated asynchronously as shown in Fig. 11(b).

4 Conclusion

In this paper, we proposed a neural segmentation model that is suitable for analog VLSIs using conventional CMOS technology. In order to facilitate the implementation of the model, instead of employing negative connections required for anti-correlated oscillation among different segments, we introduced

positive connections between activators and inhibitors among different neuron units. Moreover, we proposed a novel segmentation method based on a symmetric spike-timing dependent plasticity (STDP). The STDP characteristics were produced by combining Reichard's correlation neural networks because they are suitable for analog CMOS implementation. We demonstrated the operation of the segmentation network through numerical simulations. In addition we proposed and evaluated basic circuits for constructing segmentation hardware. We showed that the circuit could produce symmetric STDP characteristics. Finally, we confirmed operations of synchronization or desynchronization of two neuron circuits by connecting them with standard synaptic circuits (single MOS transistors). Our next target is to set up the entire segmentation network.

Acknowledgments

This study was partly supported by the Industrial Technology Research Grant Program in '04 from New Energy and Industrial Technology Development Organization (NEDO) of Japan, and a Grant-in-Aid for Young Scientists [(B)17760269] from the Ministry of Education, Culture Sports, Science and Technology (MEXT) of Japan.

References

1. Han, S.K., Kim, W.S., Kook, H.: Temporal segmentation of the stochastic oscillator neural network. Physical Review E 58, 2325–2334 (1998)
2. von der Malsburg, Ch., Buhmann, J.: Sensory segmentation with coupled neural oscillators. Biological Cybernetics 67, 233–242 (1992)
3. von der Malsburg, Ch., Schneider, W.: A neural cocktail-party processor. Biological Cybernetics 54, 29–40 (1986)
4. Wang, D.L., Terman, D.: Locally excitatory globally inhibitory oscillator networks. IEEE Trans. on Neural Networks 6(1), 283–286 (1995)
5. Ando, H., Morie, T., Nagata, M., Iwata, A.: An Image Region Extraction LSI Based on a Merged/Mixed-Signal Nonlinear Oscillator Network Circuit. In: European Solid-State Circuits Conference (ESSCIRC 2002), Italy, September 2002, pp. 703–706 (2002)
6. Reichardt, W.: Principles of Sensory Communication, p. 303. Wiley, New York (1961)
7. Asai, T., Kanazawa, Y., Hirose, T., Amemiya, Y.: Analog reaction-diffusion chip imitating the Belousov-Zhabotinsky reaction with Hardware Oregonator Model. International Journal of Unconventional Computing 1(2), 123–147 (2005)
8. Tovar, G.M., Fukuda, S.E., Asai, T., Hirose, T., Amemiya, Y.: Neuromorphic CMOS circuits implementing a novel neural segmentation model based on symmetric STDP learning. In: 2007 International Joint Conference on Neural Networks, Florida, USA, August 12-17 (2007)
9. Asai, T., Ohtani, M., Yonezu, H.: Analog MOS circuits for motion detection based on correlation neural networks. Japanese Journal of Applied Physics 38(4B), 2256–2261 (1999)