A MOS Circuit for Depressing Synapse and its Application to Contrast-Invariant Pattern Classification and Synchrony Detection

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Abstract— **A compact complementary metal-oxide semiconductor (CMOS) circuit for depressing synapses is designed for demonstrating applications of spiking neural networks for contrast-invariant pattern classification and synchrony detection. Although the unit circuit consists of only five minimum-sized transistors, they emulate fundamental properties of depressing synapses. The results of the operations are evaluated by both experiments and simulation program with integrated circuit emphasis (SPICE).**

I. INTRODUCTION

Silicon circuits that mimic the nervous systems of insects and other animals represent the future of neurocomputing. They can perform various neural functions because the microstructures of a nervous system are replicated on their silicon chips. A number of neural chips have been developed; e.g., silicon neurons that emulate cortical pyramidal neurons [1], FitzHugh-Nagumo neurons with negative resistive circuits [2], and artificial neuron circuits based on by-products of conventional digital circuits [3], [4], [5]. Since recent functional models of spiking neural networks tend to use integrate-and-fire neurons (IFNs), neuromorphic engineers have developed hardware neural systems with several types of IFN circuits to investigate the effect of spike timing and synchrony on the network's computational properties.

In addition to the IFNs, dynamic synapses have also attracted the attention of neuromorphic engineers who focus mainly on the dynamic implications of the neurons. Senn showed that an easy way to extract coherence information among cortical neurons by projecting spike trains through depressing synapses onto a postsynaptic neuron [6]. Moreover, a recent model of the layer IV circuitry, which accounts for several contrast-dependent nonlinearities in cortical responses, suggests that synaptic depression contributes to solving the problem of contrast-invariant orientation tuning [7]. Based on this suggestion, Bugmann showed that the strength of a time-averaged current injected into the soma by using a spike train is independent of its frequency, which implies that the response strength of a target neuron depends only on the number of active inputs [8].

Several CMOS circuits that emulate dynamic synapses have been developed [9], [10]. These circuits employed capacitors to obtain temporal properties of the dynamic synapse,
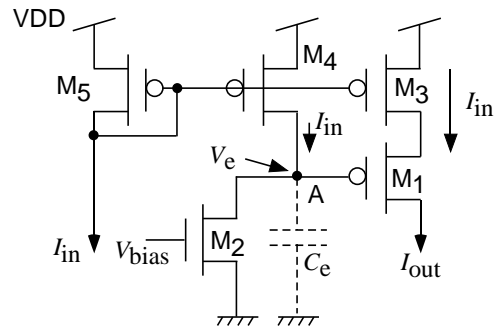

Fig. 1. Depressing synapse circuit that consists of five minimum-sized transistors and a parasitic capacitance.

which prevents us from large-scale implementation of synaptic circuits for practical applications. In this paper, we propose a compact CMOS circuit that emulate depressing properties of dynamic synapses. The circuit consists of five transistors without capacitors. We also exhibit network circuits implementing the Bugmann's model for contrast-invariant pattern classification [8] and Senn's model for synchrony detection [6], to demonstrate the properties of our synaptic circuit.

II. ANALOG CMOS CIRCUIT FOR DEPRESSING SYNAPSE

A synapse whose conductivity changes based on the firing rate or spike timing of presynaptic neurons is called a dynamic synapse [11], [12]. The change in weight of dynamic synapses is caused by short-term changes in the transmitter discharge and regeneration cycle at the terminal of presynapses rather than by learning on a network level. These synapses produce excitatory postsynaptic potential (EPSP) and inhibitory postsynaptic potential (IPSP) by integrating the output of the presynaptic neurons. A signal is conducted to a postsynaptic neuron through EPSP and IPSP. When the firing rate of the presynaptic neurons increases so that the sequential changes in EPSP and IPSP can no longer follow the input, the efficiency of signal conduction to the postsynaptic neurons drops. Thus, this synapse behaves as a low-pass filtering device. Because presynaptic neuron output is depressed and conducted to the postsynaptic neurons, such a synapse is called a "depressing synapse" and a synapse acting inversely is called a "facilitating synapse".
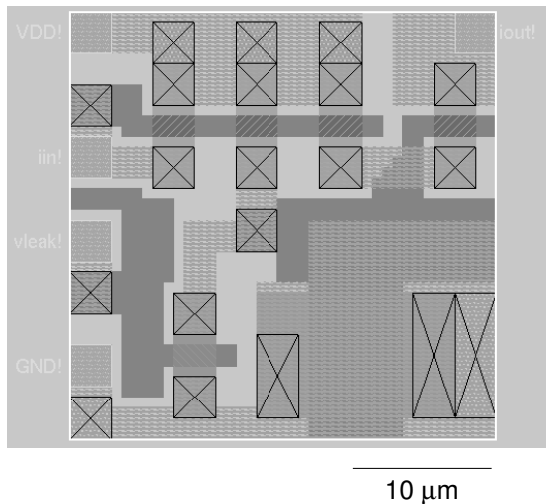
Fig. 2.   IC layout of the depressing synapse circuit (a total area of 35 μm × 36 μm with a 1.5-μm scalable CMOS rule).
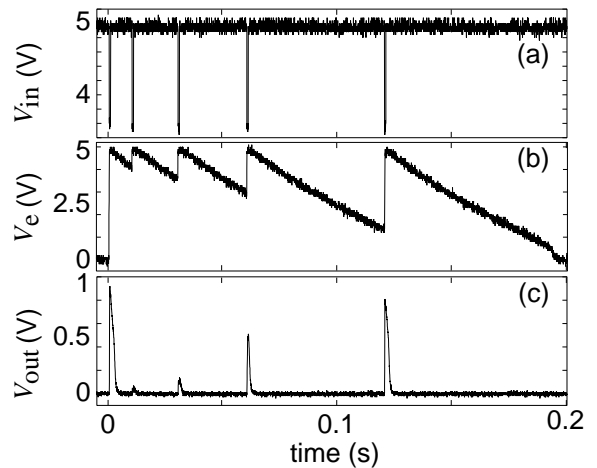

Fig. 3.   Experimental results of depressing synapse circuit; (a) successive spike inputs, (b) the degree of synaptic depression, and (c) its outputs.

Figure 1 shows our MOS circuit for such a depressing synapse constructed by a current mirror (M_3 and M_5) and pMOS common-source amplifier (M_2 and M_4). When there is no input ($I_{in} = 0$), voltage V_e at junction A is zero because of leak transistor M_2. Therefore, transistor M_1 is in an on state. When there is input ($I_{in} > 0$) that increases V_e, M_1 enters an off state. Therefore, the current is mirrored to output I_{out} through transistor M_1.

Because there is parasitic capacitance C_e at junction A, the increase in V_e has a short-time delay. Therefore, M_1 enters an on state for a short time, and the circuit outputs pulsive current I_{out}. When the input current becomes zero again, M_2 discharges the capacitance C_e, and V_e returns to zero. Remarkably, the Mirror effect of the pMOS common-source amplifier, which amplifies the value of additional parasitic capacitance between the drain and gate terminal of M_2, increases this discharging time.

Now assume that the pulsive current (spike) is given at a short interval, and that subsequent spikes enter before V_e returns to zero. In this case, the amplitude of the output spikes decreases when V_e increases. Because the current of transistor M_2 increases monotonically when V_{bias} increases, the time until V_e returns to zero decreases. By adjusting voltage V_{bias}, it is thus possible to change the time of the depression. Note that, when V_{bias} is set at VDD, the circuit behaved as a nondepressed synapse because V_e is zero and M_1 is always in an on state.

III. EXPERIMENTAL AND SIMULATION RESULTS

We fabricated a prototype circuit using a 1.5-μm scalable CMOS rule (MOSIS, vendor: AMIS, n-well single-poly double-metal CMOS process). Figure 2 shows a layout of the depressing-synapse circuit. The circuit took up a total area of 35 μm × 36 μm.

Figure 3 shows time courses of the output of the synapse circuit for increasing input-spike intervals. The experimental
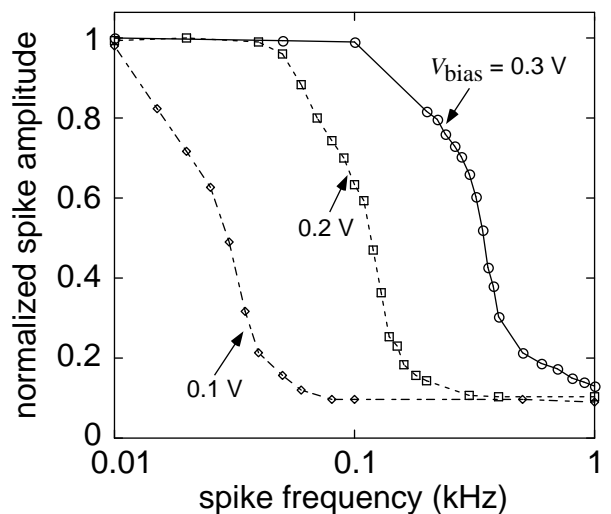
Fig. 4.   Changes in amplitude of the output of depressing synapse circuit against the firing rate of presynaptic neuron.

conditions were VDD = 5 V, V_{bias} = 0.1 V, input spike width = 0.1 ms and spike amplitude = 1 μA. A load resistance of 100 MΩ was connected between the output terminal of the circuit and ground to obtain the output current I_{out} as the voltage V_{out}. Figure 3(a) shows input voltage V_{in} of transistors $M_3 \sim M_5$ that decreases from 5 V to 3.7 V when the spike current is given. The first spike was given at $t = 0$. Subsequent spikes were given at t = 10, 30, 60 and 120 ms. When the inputs were given successively in a short time (around 0 to 30 ms in Fig. 3(a), the amplitude of the output pulse was depressed [Fig. 3(c)]. As the interval widened, V_e approached zero [Fig. 3(b)], and the amplitude of the output pulse returned to the initial value.

Figure 4 shows the change in amplitude of the output spike against the input firing rate. The leak voltage V_{bias} was set at 0.1, 0.2, and 0.3 V. As the spike frequency increases, the amplitude of the output pulse decreased. By increasing V_{bias},
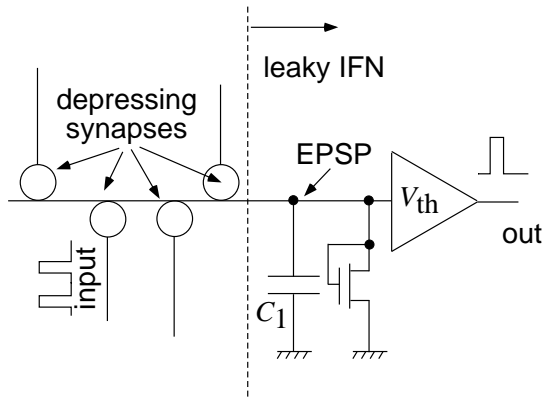
Fig. 5. Experimental setups for pattern classification and synchrony detection.
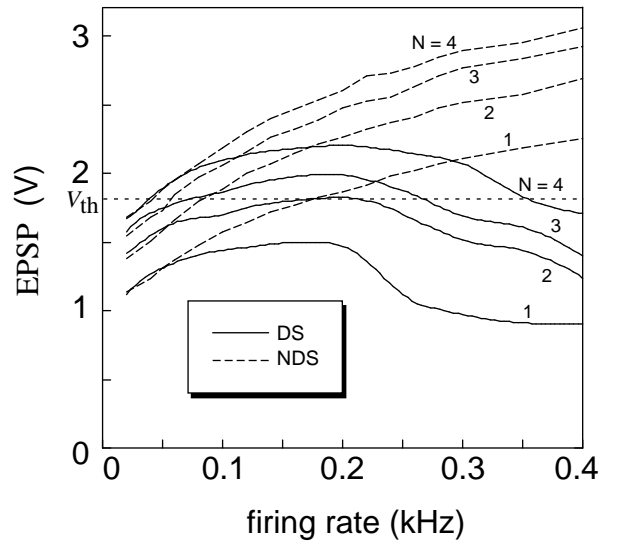

Fig. 6. Changes in EPSP of IFN against the number of active presynaptic neuron and their firing rates.

Fig. 7. Results for dependence of IFN on the firing rate of presynaptic neurons (4 neurons).

the cutoff frequency was successfully shifted toward the higher frequency.

In the following subsections, we show applications of the proposed circuit to spiking neural networks for contrast-invariant pattern classification and synchrony detection. Although these networks are designed to be useful when large number of depressing synapses are employed, we constructed small-scale circuits to demonstrate only fundamental properties of the hardware neural networks. Since our circuit occupies an area of 35 μm $\times$ 36 μm even if we use 1.5-μm CMOS process, its large-scale implementation is remarkably easy.

A. Application to the Bugmann's Neural Network for Contrast-Invariant Pattern Classification

Bugmann showed that the strength of a time-averaged current injected into the soma by using a spike train tends to be independent of its frequency, which implies that the response strength of a target neuron depends only on the number of active inputs [8]. We here demonstrate it by using our depressing synapse circuits.

Let us assume a simple circuit, as shown in Fig. 5. The circuit is designed based on the construction of Bugmann's neural network. The right part represents a leaky IFN and the left part represents its dendrite. The IFN consists of a membrane capacitance (C_1), a diode-connected leak MOS transistor and a threshold detector (V_{th}). The IFN accepts spike inputs from excitatory neurons through depressing synapses. The IFN outputs a spike when its EPSP $> V_{th}$, and resets the EPSP after the firing. In this setup, average values of the EPSP increases in proportion to the number of presynaptic active neurons. Therefore, it can detect the number of presynaptic active neurons by setting appropriate threshold V_{th} corresponding to the number of active neurons. On the other hand, the EPSP also increases in proportion to firing rate of spiking neurons. Therefore, the performance to discriminate the number of presynaptic active neurons largely deteriorates if the firing rate is not constant value.

It is shown that this discrimination performance is improved by using the depressing synapse [8]. If input spikes are given
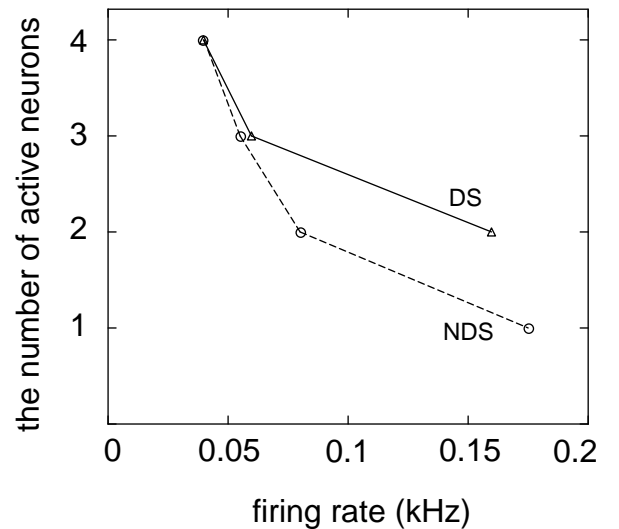
to the depressing synapse successively in a short period, the efficiency to increase the EPSP per spikes drops. Even if the number of input spikes increases with the increase in firing rate, the value of EPSP does not change greatly because the efficiency per spike is lowered by the synaptic depression. Namely, the discrimination performance of the network tends to be independent of firing frequency. To demonstrate this, we construct a network in which four synapse circuits are connected to the IFN circuit. We compared the operation of the neuron circuit with nondepressed- and depressed circuit as the number of active presynaptic neurons increases (Fig. 6). In the figure, N represents the number of active inputs. In case of the nondepressed synapse ($V_{bias} = 5$ V, and it is labeled as NDS in the figure), average value of the EPSP increased monotonically

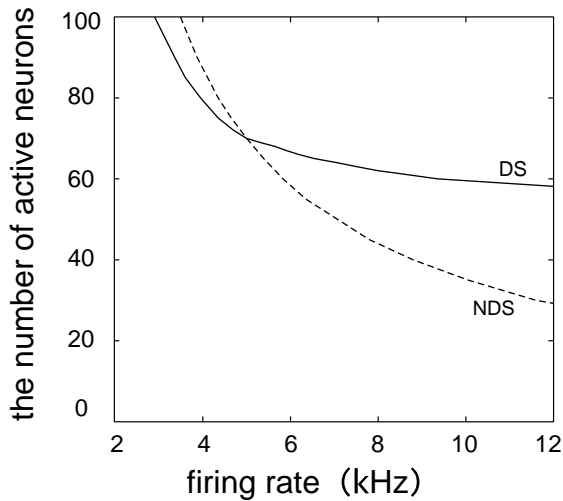Fig. 8. Large-scale simulation results (100 neurons) for the same experiments shown in Fig. 7.

Fig. 9. Responses of EPSP for single burst input (a) via nondepressed (b) and depressed synapse circuit (c).

as the firing rate of postsynaptic neurons increased. The value also increased as N increased. On the other hand, in case of the depressed synapse ($V_{\text{bias}} = 0.2$ V, and it is labeled as DS in the same figure), the EPSP increased nonmonotonically as the firing rate of postsynaptic neurons increased. Now, we define the firing threshold of the IFN as $V_{\text{th}} = 1.8$ V. The firing rates when the EPSP exceeded the threshold to the number of active neurons were plotted in Fig. 7 for both depressed (DS) and nondepressed (NDS) synapse circuits. The result indicates that the dependence of the postsynaptic neuron with depressed synapses on presynaptic firing rates is smaller than that of nondepressed synapses.

This difference becomes more apparent when N increases. To confirm it in a large-scale network, SPICE simulation was conducted for the network having 100 synapses. As input, pulse with pulse amplitude of 1 nA and pulse width of 10 μs was given. The time constant of postsynaptic neuron was set around 2 ms. The threshold was set at the value of the EPSP produced by 70 active neurons with a firing frequency of 5 kHz. The values of threshold V_{th} were 0.2 V when the depressing synapse was used and 2.0 V when conventional synapse was used. The result is shown in Fig. 8. The firing rate when the EPSP exceeded the threshold to the active neuron for the first time were plotted.

Let us assume that presynaptic active neurons are arranged on 2D rectangular grid and forms some patterns; e.g., "E", "L" or "-", and "E" is with 90 active neurons, "L" with 50, and "-" with 10. Then, suppose that the firing rate of the active neurons represents the "contrast" strength of these patterns. If there is little dependence on the presynaptic firing rates, the neuron can classify these patterns independent of their contrast strength. The result shown in Fig. 8 indicates that in using depressing synapse, correct classification can be achieved for all patterns.
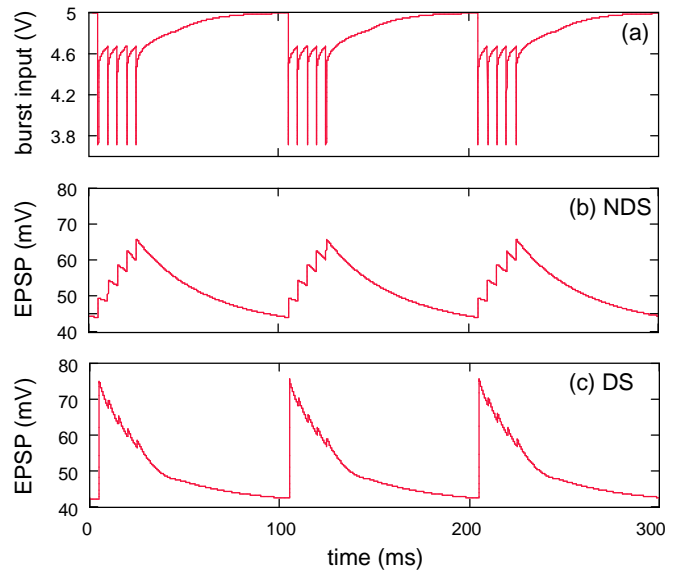
B. Application to the Senn's neural network for synchrony detection

Senn showed that an easy way to extract coherence information among cortical neurons by projecting spike trains through depressing synapses onto a postsynaptic neuron [6]. We here demonstrate it by using our depressing synapse circuits.

Let us consider the same IFN as shown in Fig. 5. We here employ burst neurons as inputs to the IFN, as in the Senn's original work. Duging a burst input, the output current of the depressing synapse circuit rapidly decreases for successive spikes due to the increase of V_{e} and its slow recovery. But during a nonbursting period, V_{e} has time to be 0, and this results in a strong EPSP at the onset of the next burst. If we compare this dynamic response with that for a nondepressed synapse evoking on average the same EPSP, the depressed synapse will have a larger response at the burst onset and a smaller response toward the end of the bursts.

Figure 9 show the response of the EPEP with bursting inputs (a) for a nondepressed synapse (b) and depressed synapse circuit (c). Amplitudes of bursting spike inputs were set at 1 μA for depressing synapses and 600 pA for nondepressed synapses, which evoked on average the same EPSP (50 mV). This result ensures that the EPSP caused by the depressed synapse circuit has a larger response at the burst onset, as compared with nondepressed synapse circuit.

Now we demonstrate that the depressing synapse circuit is able to detect the synchrony in the burst times. We employ two bursting neurons as the input of the IFN that receive the burst inputs through depressed or nondepressed synapses. Figures 10 and 11 show the results. When the input bursts are not synchronized [Figs. 10(a) and (b)], the peak EPSPs evoked by nondepressed [Figs. 10(c)] and depressed synapses [Figs. 10(d)] were both around 0.1 V. But, when the input bursts are synchronized [Figs. 11(a) and (b)], the peak EPSP
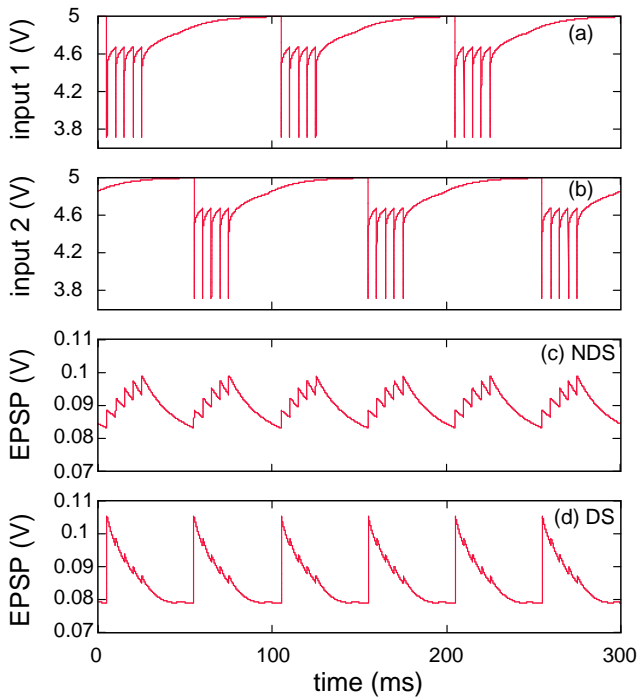
Fig. 10. Responses of EPSP for asynchronous burst inputs [(a) and (b)] via nondepressed (c) and depressed synapse circuit (d).

Fig. 11. Responses of EPSP for asynchronous burst inputs [(a) and (b)] via nondepressed (c) and depressed synapse circuit (d).

evoked by depressed synapses [Figs. 11(d)] was significantly larger than the nodepressed synapses [Figs. 11(c)]. Therefore, defining an appropriate threshold V_{th} of the IFN; e.g., V_{th} = 130 mV in the experiments, the IFN with the depressing synapse circuit can fire when the burst inputs are synchronized.

Next, we simulated the output of 100 neurons by random spike trains (Fig. 12a). According to [6], there is experimental evidence to assume that before and during the tone, auditory cortical neurons fire in short bursts with bursts of three to four spikes within 40-50 ms, repeated every 200-250 ms. During the tone, the burst onsets are assumed to be synchronized within groups of 70 neurons that are randomly assembled anew for each burst. In our simulations, the overall firing rate of the population remains constant, apart from the short onset and offset of the tone when most cells burst together because the bursting times of the groups alternate during the ongoing tone (see Fig. 12b).

Applying a tone stimulus (20-45 ms in Fig. 12), the neurons respond at the onset and offset. They correlate their bursts only among randomly assembled subgroups during the stimulus. Since the mean firing rate is on the background level during the tone (Fig. 12b), a postsynaptic neuron gathering the input spike trains through nondepressed synapses would respond only at the stimulus onset and offset. With depressing synapses, however, the postsynaptic neuron detects the correlated bursts and fires during the tone as well (Figs. 12c and 12d), as shown in the Senn's original work.

To investigate noise tolerance of Senn's network with the proposed circuits, we simulated the 100 neuron network with random-scattering devices. In this simulation, the threshold
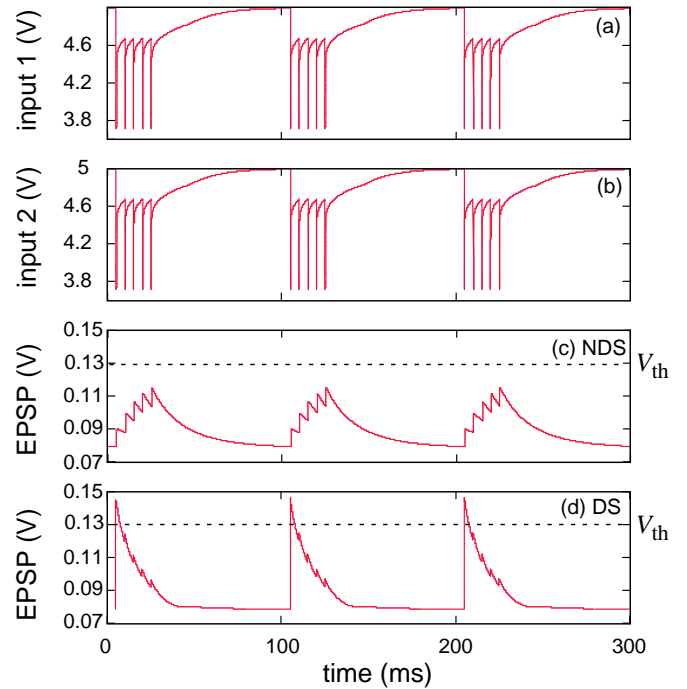
voltage of each MOS transistor was scattered by Gaussian noise with standard deviation σ. To evaluate the noise tolerance, we counted the number of spikes of the presynaptic neuron during bursting and non-bursting period (Fig. 13). Ideally, the postsynaptic neuron must not fire during non-bursting period but must fire during bursting period, for the task of synchrony detection. The difference between the number thus represent the performance of this task. The number of postsynaptic spikes increased as the increase of σ during bursting period. On the other hand, when $\sigma > 25$ mV, the postsynaptic neuron started firing suddenly. Namely, the performance of synchrony detection did not change significantly by the increase of σ as long as $\sigma < 25$ mV. Remarkably, the difference ($\sim$ performance of synchrony detection) changed nonmonotonically as the increase of σ, as shown in Fig. 14.

IV. CONCLUSION

We designed and fabricated an electronically implemented depressing synapse. The circuit was designed by using only five minimum-sized transistors, and did not use any capacitor to make its temporal property. As the result, the circuit took up a total area of 35 μm $\times$ 36 μm with a 1.5-μm scalable CMOS rule (MOSIS, vendor: AMIS, n-well single-poly double-metal CMOS process). By using the synapse circuit, we demonstrated two functional neural networks performing contrast-invariant pattern classification and synchrony detection. The results indicated that the depressing synapse circuit worked well on these networks in actual environment with realistic configurations, and suggested further potential applications to large-scale spiking neural networks with depressed and
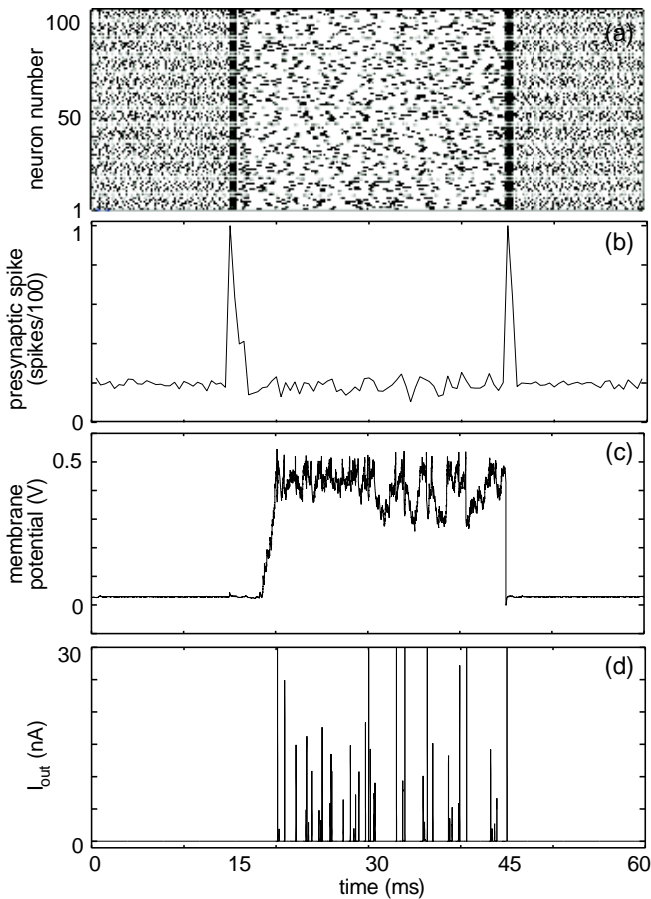
Fig. 12. Simulation results of 100-neuron network stimulated by random spike trains through depressing synapses.

Fig. 13. Change of the number of spikes of the presynaptic neuron during bursting and non-bursting period as function of standard deviation σ of MOS transistor's threshold voltage.

Fig. 14. Change of the difference between the number of spikes of the presynaptic neuron during bursting and non-bursting period as function of σ.

nondepressed synapses.

ACKNOWLEDGEMENT

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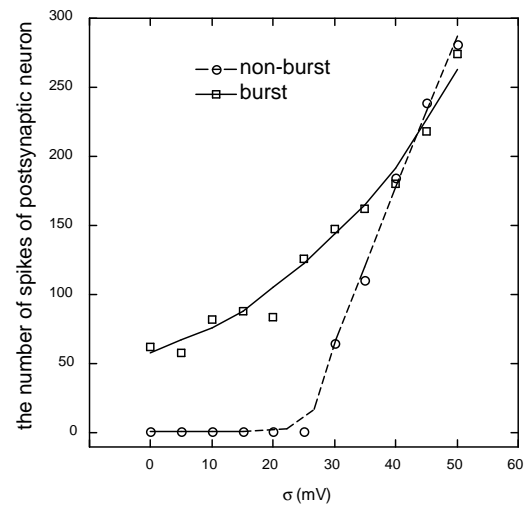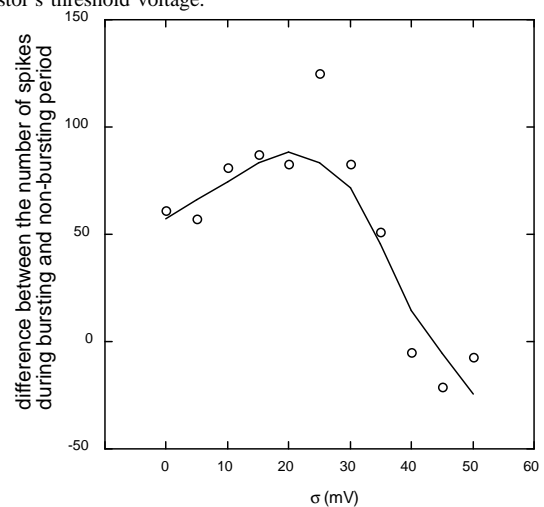
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