AN ANALOG CMOS CHIP IMPLEMENTING A CNN-BASED LOCOMOTION CONTROLLER FOR QUADRUPED WALKING ROBOTS

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ABSTRACT

We propose an analog CMOS circuit that implements a class of cellular neural networks (CNNs) for locomotion control in robotics. Our circuit is constructed using multiple-input floating-gate MOS (FGMOS) FETs aiming at the voltage-mode operation, and it can be expected to reduce power consumption. Furthermore, we fabricated a prototype chip using a standard CMOS process. From experimental results, we have confirmed that the proposed circuit has capability of generating stable rhythmic patterns for robot locomotion control under an actual environment.

1. INTRODUCTION

Biologically inspired approaches have succeeded in motion control in robotics. Biological systems have been evolved to optimize themselves under selective pressures for a long time, and thus it is expected that biological findings provide us valuable ideas for design and control methods in robotics.

Central pattern generator (CPG) is the biological neural network that can produce rhythmic movements for locomotion of animals, such as walking, running and swimming [1]. A CPG consists of sets of neural oscillators, situated in ganglion or spinal cord. Induced inputs from command neurons, the CPG generates a rhythmic pattern of neural activity, resulting in a rhythmic movement for locomotion of animals. Such a rhythmic movement induces coordination of physical parts. Since the degree of freedom relevant to locomotion is very high, this coordination is necessary for stable locomotion. Therefore, CPG can be said to play the principle role in locomotion of animals.

During the past decade, many researchers have designed locomotion controllers based on the CPG framework [2]-[3]. Such controllers have the advantages in i) reduction of the amount of calculation required for locomotion control because of needless of complicated planning for generating motion trajectory, and ii) high adaptation to an unexpected disturbance as a result of a CPG interacting with environments through sensory information.

Recently, Arena *et al.* have proposed a class of cellular neural networks (CNNs) as a CPG controller in a hexapod robot [4]. In general, a CNN is an analog dynamic processor array with locally connections, and therefore it can perform parallel and distributed processing, and continuous time and value signal processing essentially. Furthermore, their CNN is a class of autonomous CNNs that can generate various spatial-temporal patterns automatically. Thus, it is suitable for a CPG contrler to generate rhythmic motion patterns for robot locomotion control in real-time.

In the present paper, we propose an analog CMOS chip that implements a class of CNN for locomotion control in quadruped walking robots. CNN-based CPG controllers have already been implemented on silicon chips [6]-[7]. In these CNN chips, the components called cells interacts with neighboring ones thorough current, and thus these chips have several problems, such as current mismatch and power consumption. In particularly, the power consumption is a critical point for long term operation. Hence, we introduce a transformed CNN, and designed it as an analog CMOS circuit using multiple-input floating-gate MOS (FGMOS) FETs aiming at the voltage-mode operation. As a result, it can be expected to reduce the bias currents, and then the amount of power consumption. Furthermore, we fabricated a first prototype chip using a standard CMOS process. From experimental results, we confirmed that the proposed circuit can operate stably under an actual environment.

2. A CNN-BASED CPG MODEL

We here propose a CNN-based CPG model for locomotion control in quadruped walking robots. In the previous works, Arena *et al.* have proposed a class of CNNs as a CPG model for locomotion control in biologically-inspired robots, such as a hexapod robot [5]-[7]. Their model is described the following equations:

$$\dot{x}^1_{i,j} = -x^1_{i,j} + (1+\mu)y^1_{i,j} - sy^2_{i,j} + S^1_{i,j} \tag{1}$$

$$\dot{x}^2_{i,j} = -x^2_{i,j} + sy^1_{i,j} + (1+\mu)y^2_{i,j} + S^2_{i,j} \tag{2}$$

with

$$S^1_{i,j} = D_1(y^1_{i-1,j}+y^1_{i+1,j}+y^1_{i,j-1}+y^1_{i,j+1}-4y^1_{i,j}) + I^1_{i,j} \quad (3)$$

$$S^2_{i,j} = D_2(y^2_{i-1,j}+y^2_{i+1,j}+y^2_{i,j-1}+y^2_{i,j+1}-4y^2_{i,j}) + I^2_{i,j} \quad (4)$$

where $x^n_{i,j}$ is a state variable, $I^n_{i,j}$ a bias constant $(n = 1, 2,$ (i, j) is a grid point of the cell), μ and s the coupling parameters, D_n a diffusive coefficient, and an output $y^n_{i,j} = f(x^n_{i,j})$, which is a nonlinear function usually given by the piecewise linear function or the sigmoid function.

The above model has been proposed as the reaction-diffusion (RD) CNN for simulator of RD partial differential equations in [4]. The RD-CNN can produce various spatial-temporal patterns automatically, and thus it is suitable for CPG controllers in generating various locomotion patterns.

Let us introduce a novel RD-CNN, which is suitable for constructing an analog CMOS circuit that operates in voltage-mode. Firstly, we rewrite (1)-(4) as follows:

$$\dot{x}^1_{i,j} = -x^1_{i,j} + \sum_{k,l} A_{i,j;k,l} y^1_{k,l} - \sum_{k,l} B_{i,j;k,l} y^2_{k,l} + I^1_{i,j} \quad (5)$$

$$\dot{x}^2_{i,j} = -x^2_{i,j} + \sum_{k,l} C_{i,j;k,l} y^1_{k,l} - \sum_{k,l} D_{i,j;k,l} y^2_{k,l} + I^2_{i,j} \quad (6)$$

where $A_{i,j;k,l}, B_{i,j;k,l}, C_{i,j;k,l}$ and $D_{i,j;k,l}$ are coupling coeficients, (k, l) is a grid point in neighborhood of the point (i, j). The above formalism is naturally extended to include the cross diffusion terms. Then, we rewrite the equations above in terms of a new state variable $v^n_{i,j}$ as follows:

$$\dot{v}^1_{i,j} = -v^1_{i,j} + f(\sum_{k,l} A_{i,j;k,l} v^1_{k,l} - \sum_{k,l} B_{i,j;k,l} v^2_{k,l} + I^1_{i,j}) \quad (7)$$

$$\dot{v}^2_{i,j} = -v^2_{i,j} + f(\sum_{k,l} C_{i,j;k,l} v^1_{k,l} - \sum_{k,l} D_{i,j;k,l} v^2_{k,l} + I^2_{i,j}). \quad (8)$$

The equations can be derived from (5) and (6) by the following transformation:

$$x^1_{i,j} = \sum_{k,l} A_{i,j;k,l} v^1_{k,l} - \sum_{k,l} B_{i,j;k,l} v^2_{k,l} + I^1_{i,j} \quad (9)$$

$$x^2_{i,j} = \sum_{k,l} C_{i,j;k,l} v^1_{k,l} - \sum_{k,l} D_{i,j;k,l} v^2_{k,l} + I^2_{i,j}. \quad (10)$$

The transformation above is an Affine, and its inverse transformation is also an Affine. Thus, (5)-(6) and (7)-(8) are dynamically equivalent. In case of $f(x) = \tanh(x)$, similarly, the above transformation can be checked. As it is shown in the following section in detail, the transformation is useful for chip implementation rather than a mathematical problem. In biological point of view, the above formalism is a special case of the Wilson-Cowan neural system whose components are only connected within their neigherhood. We are going to consider the transformed CNN given by (7)-(8) as the CPG model for constructing a CPG controller.

3. CIRCUIT ARCHITECTURE

We here propose an analog CMOS circuit that implements a CNN-based CPG controller. First, we have designed a cell circuit that constitutes a part of the proposed CNN, which consists of four analog elementary circuits, differential pair, current mirror, RC circuit and current source (Fig.1(a)).

The differential pair, which is the most fundamental components of the cell circuit, can approximate the sigmoidal function. When the MOS FETs comprising the differential pair operate in their subthreshold region, the static response of the differential pair is represented as:

$$I_\mu(V^+ - V^-) = I_b \frac{1 + \tanh(\mu(V^+ - V^-))}{2} \quad (11)$$

where I_μ is the output current of the differential pair, V^+ and V^- the input voltages, I_b the bias current, $\mu = \kappa/2V_T$, V_T the thermal voltage and κ the electrostatic coefficient between the gate and channel. By subtracting a half of the bias current from the output current I_μ, the characteristic of the nonlinear function $f(x)$ is obtained.

Furthermore, we replace the MOS FETs that comprise the differential pair with multiple-input FGMOS FETs [8] (Fig. 1(b)). As a result, the operation of weighted linear summation of voltages is realized. Generally, the floating-gate voltage of the multiple-input FGMOS FET is expressed by the following equations [8]:

$$V_{FG} = \frac{C_{GD}}{C_T} V_D + \frac{C_{GS}}{C_T} V_S + \frac{C_{GB}}{C_T} V_B + \frac{Q_0}{C_T} + \sum_l \frac{C_l}{C_T} V_l \quad (12)$$

where $C_T = C_{GD} + C_{GS} + C_{GB} + \sum_l C_l$ and V_l are the input gate voltages, C_l the capacitances between each of the input gates and the floating-gate, and Q_0 represents any initial charge in the floating-gate. The floating-gate voltage approximately expressed by:

$$V_{FG} \simeq \sum_l \frac{C_l}{C_T} V_l \quad (13)$$

where it is assumed that Q_0 is 0 and $C_{GD}, C_{GS}, C_{GB} \ll C_T$. Then, the differential voltages between the floating-gates of the differential pair with multiple-input FGMOS FETs is approximately expressed by the following equations:

$$V^+_{FG} - V^-_{FG} \simeq \sum_l \frac{C^+_l}{C_T} V^+_l - \sum_l \frac{C^-_l}{C_T} V^-_l \quad (14)$$

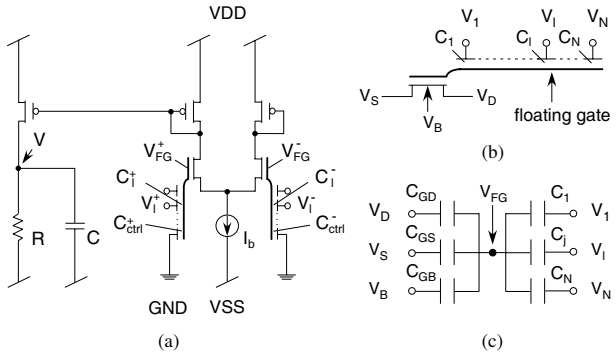


Fig. 1. Schematic of cell circuit.

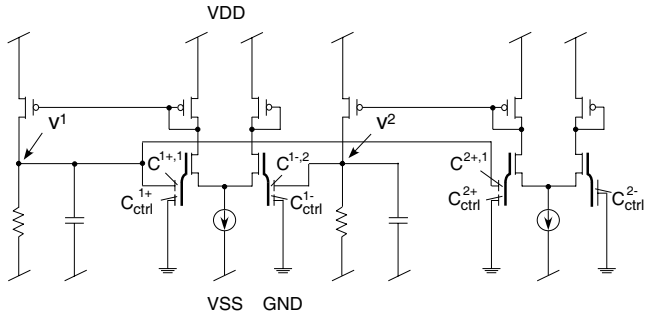


Fig. 2. Schematic of unit circuit.

where V_{FG}^{+} and V_{FG}^{-} are the floating-gate voltages, V_l^{+} and V_l^{-} the input gate voltages, C_l^{+} and C_l^{-} the capacitances between each of the input gates and the floating-gate.

After the output current of the differential pair, I_μ, is reversed by current mirror, it is integrated by RC circuit. The circuit dynamics is represented as:

$$C\dot{V} = -\frac{V - V_{SS}}{R} + I_\mu(V_{FG}^{+} - V_{FG}^{-}) \tag{15}$$

where C is the capacitance and R the resistance. We set that substrate voltage $V_{SS} < 0$ for the purpose of setting the equilibrium voltage at 0. When we assumed that $V_{SS}/R + I_b/2 = 0$, the equation above is rewritten as follows:

$$C\dot{V} = -\frac{V}{R} + \frac{I_b}{2}\tanh(\mu(V_{FG}^{+} - V_{FG}^{-})) \tag{16}$$

$$\simeq -\frac{V}{R} + \frac{I_b}{2}\tanh(\mu(\sum_l \frac{C_l^{+}}{C_T}V_l^{+} - \sum_l \frac{C_l^{-}}{C_T}V_l^{-})) \tag{17}$$

$$= -\frac{V}{R} + \frac{I_b}{2}F_\mu(\sum_l C_l^{+}V_l^{+} - \sum_l C_l^{-}V_l^{-}) \tag{18}$$

where we have replaced $F_\mu(x) = \tanh(\mu x/C_T)$.

We constructed an unit circuit from two cell circuits. Figure 2 shows schematic of the unit circuit, where V^1 and V^2 represent the volatege of the first cell and the second cell, respectively. This circuit has reciprocal interactions via capacitive coupling.

Furthermore, we constructed the entire network circuit from four unit circuits. The network dynamics is given by the following equations:

$$C\dot{V}_{i,j}^{1} = -\frac{V_{i,j}^{1}}{R} + \frac{I_b}{2}F_\mu(\sum_{k,l,n} C_{k,l;i,j}^{1+,n}V_{k,l}^{n} - \sum_{k,l,n} C_{k,l;i,j}^{1-,n}V_{k,l}^{n}) \tag{19}$$

$$C\dot{V}_{i,j}^{2} = -\frac{V_{i,j}^{2}}{R} + \frac{I_b}{2}F_\mu(\sum_{k,l,n} C_{k,l;i,j}^{2+,n}V_{k,l}^{n} - \sum_{k,l,n} C_{k,l;i,j}^{2-,n}V_{k,l}^{n}) \tag{20}$$

where $V_{i,j}^{1}$ and $V_{i,j}^{2}$ represent the volatege of the first cell and the second cell, respectively. The total capacitance of the floating gate C_T is given by $C_T = C_{GD} + C_{GS} + C_{GB} + \sum_{k,l,n} C_{i,j;k,l}^{m\pm,n} + C_{ctrl,i,j}^{m\pm}$ $(m,n = 1,2)$, where $C_{ctrl,i,j}^{m\pm}$ is the capacitance of each of the control gates, which is added to control the total capacitance of the floaring-gate.

Depending on its coupling structure, the network circuit generates different rhythmic patterns. Figures 3(a)-(c) show the network structures that generate rhythmic patterns corresponding to the locomotion patterns, such as walk, trot and gallop, respectively. Here, the grid points $(1,1)$, $(1,2)$, $(2,1)$ and $(2,2)$ correpond to each limb of mammals.

4. EXPERIMENTAL RESULTS

We fabricated a first prototype chip using a standard CMOS process (MOSIS AMIS 1.5-μm) excepting the RC circuits. For constructing the RC circuits, we used off-chip resistors and capacitors. By experiments on the fabricated chip, we confirmed the operation of the proposed circuit. First, we set common parameters: the capacitance $C = 1.0$ μF, the resistance $R = 1.0$ MΩ, the bias current $I_b = 3$ μA, the coupling capacitances:

$$C_{i,j;i,j}^{1+,1} = C_{i,j;i,j}^{1-,2} = 0.5,\ C_{i,j;i,j}^{2+,1} = 0.3, C_T = 1.0\ \text{pF}$$

and the voltages $V_{DD} = 1.5$ V and $V_{SS} = -1.5$ V. Then, we removed initial floating-gate charges by UV shining.

After that, we measured voltages in the fabricated chip under a noisy environment (SNR: 30dB). Figures 4(a) and (b) show waveforms of voltages $V_{i,j}^{1}$ in both walk mode and trot mode shown in Figs. 3(a)-(b). Here LF, RF, LH and RH represent left forelimb, right forelimb, left hindlimb and right hindlimb of mammals, respectively.

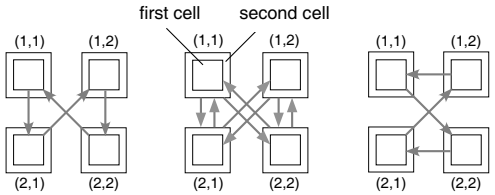
In the walk mode, we set the coupling capacitance as:

$$C_{1,1;2,2}^{1-,1} = C_{1,2;2,1}^{1-,1} = C_{2,1;1,1}^{1-,1} = C_{2,2;1,2}^{1-,1} = 0.1\ \text{pF}$$

and the others were set at 0 F.

In the trot mode, we set the coupling capacitance as:

$$C_{1,1;2,2}^{1-,2} = C_{1,2;2,1}^{1-,2} = C_{2,1;1,2}^{1-,2} = C_{2,2;1,1}^{1-,2} = 0.1\ \text{pF}$$
$$C_{1,1;2,1}^{2-,2} = C_{1,2;2,2}^{2-,2} = C_{2,1;1,1}^{2-,2} = C_{2,2;1,2}^{2-,2} = 0.2\ \text{pF}$$



(a) Walk mode. (b) Trot mode. (c) Gallop mode.

Fig. 3. Coupling configurations of network circuits.

and the others were set at 0 F.

If we assume that $V^1_{1,1}, V^1_{1,2}, V^1_{2,1}$ and $V^1_{2,2}$ drive LF, RF, LH and RH, respectively, and then such rhythmic patterns are considered as typical locomotion patterns of mammals.

Furthermore, we estimated power consumption of the chip during operation by approximating the waveforms of the measured voltages as sinusoidal waves. In a steady state, the amount of the electrical power was about 140 μW.

The results show that the CNN chip can generate stable rhythmic patterns corresponding to the typical locomotion patterns of animals under noisy environments, and reduce power consumption during operation. Such characteristics of the CNN chip are suitable for locomotion control in a quadruped walking robot in real situations.

5. CONCLUSIONS

We have fabricated an analog CMOS chip that implements a CNN-based CPG controller. In the past, CNN-based CPG controllers have already been implemented on silicon chips [6]-[7]. For instance, Branciforte *et al.* have proposed an analog CMOS chip that operates in current-mode [6]. Their chip is constructed from many current amplifiers, and then it has good programability. However, it is difficult to operate stably without tuning bias currents because of irregularity in currents thorough the current amplifiers. Arena *et al.* have presented a hybrid VLSI chip, which is designed based on the operational amplifier implementation of the CNN cell [5] and the switched-capacitor technique [7]. Their chip has the advantages in controlling of its operation speed. In these chips, the cells are interaction thorough currents, and thus these chips have several problems, such as current mismatch and power consumption. In contrast, our chip has been designed using multiple-input FGMOS FETs aiming at the voltage-mode operation. As a result, the chip can generate stable rhythmic patterns for robot locomotion control under actual environment with low power consumption.

6. REFERENCES

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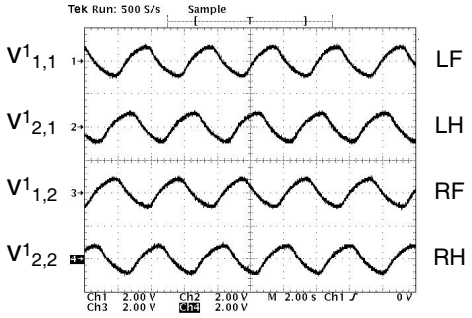
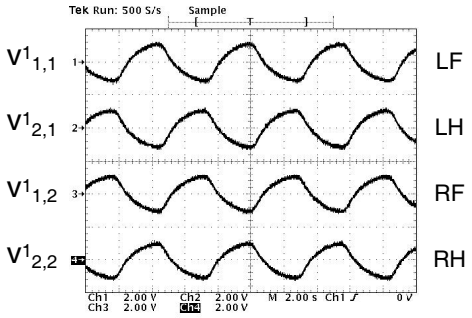


(a) Walk mode.



(b) Trot mode.

Fig. 4. Waveforms of voltages in network circuits.

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