Floating millivolt reference for PTAT current generation in Subthreshold MOS LSIs

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***Abstract*— A floating millivolt reference circuit to generate a PTAT current was developed by using MOSFETs operated in the subthreshold region. The circuit generates a floating voltage of about 10 mV. The variations in the reference are ±2.7 % in a temperature range from –20 to 100 ℃. The accuracy of the reference circuit can be improved to ±0.3 % with a correction technique using a curvature-correction circuit. The total power consumption of the circuit was 4.6 μW at 100 ℃.**

I. Introduction

Intelligent-network systems with various smart-sensor devices are expected to be developed that will spread all over the world to enable infrastructures to be constructed for the information age. Such network systems will require a huge number of sensor LSIs that measure various physical data from our surroundings, store and process these measured data, and output them on demand. As these sensors must operate for long periods of time, the available energy resources –whether small batteries, energy harvesting, or both– limit their overall operation. One possible method of minimizing the energy they consume is to design a circuit in the subthreshold region of MOSFETs.

The sensing of temperature by these LSIs is one of their most fundamental applications. A sensory signal that is proportional to absolute temperature (PTAT) is necessary to construct a temperature sensor. However, as the subthreshold current of MOSFET is an exponential function of the gate-source voltage, the PTAT current cannot be generated easily. In this paper, we propose a floating millivolt reference circuit that can be used to generate PTAT current in circuits [1]. In the following, Section II describes the method of generating PTAT current for the temperature sensor, Section III presents the floating millivolt reference with the results of SPICE simulation, and Section IV describes the curvature-correction techniques to obtain a high-accuracy reference.

II. Generation of PTAT Current

The subthreshold current I_D of a MOSFET is an exponential function of gate-source voltage V_{GS} and is given by

$$I_D = I_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right), \tag{1}$$

where I_0 is a process-dependent parameter, η is the subthreshold slope factor, and $V_T (= k_B T/e)$ is the thermal voltage [2].

Assume that two MOSFETs are biased with two different voltages V_{GS1} and V_{GS2} to generate two subthreshold currents I_{D1} and I_{D2}. The difference in the current ratios is given by

$$\frac{I_{D2}}{I_{D1}} - \frac{I_{D1}}{I_{D2}} = \exp\left(\frac{V_{GS2} - V_{GS1}}{\eta V_T}\right) - \exp\left(-\frac{V_{GS2} - V_{GS1}}{\eta V_T}\right). \tag{2}$$

Equation (2) can be rewritten for a voltage difference of $|V_{GS2} - V_{GS1}| < \eta V_T$ as

$$\frac{I_{D2}}{I_{D1}} - \frac{I_{D1}}{I_{D2}} = 2\frac{V_{GS2} - V_{GS1}}{\eta V_T}. \tag{3}$$

The reciprocal of Eq. (3) is expressed as

$$\frac{1}{\frac{I_{D2}}{I_{D1}} - \frac{I_{D1}}{I_{D2}}} = \frac{\eta V_T}{2(V_{GS2} - V_{GS1})} = \frac{\eta k_B}{2e(V_{GS2} - V_{GS1})} T. \tag{4}$$

The PTAT characteristic can be obtained for a fixed temperature-independent voltage difference of $|V_{GS2} - V_{GS1}|$.

In practical circuit implementation, the division and the subtraction of the currents can be performed by translinear circuit and current mirror circuit [1]. However, generating a small temperature-independent floating reference voltage ($\sim$ 10 mV) to generate the PTAT signal in Eq. (4) is not easy using a MOSFET operated in the subthreshold region. In the following sections, we develop a floating millivolt reference circuit.

III. Floating Reference Circuit

A. Circuit Configuration

A bandgap reference circuits are widely used to obtain a constant reference voltage and a floating reference voltage [3]. However, they are not suitable for our purpose because they need large resistors with high resistance for low-current operation in the subthreshold region. Buck and others proposed a new CMOS bandgap reference circuit without the use of resistors [4]. We modified their circuit to operate in the subthreshold region and to generate a floating millivolt reference.

Figure 1 shows the circuit configuration. The circuit consists of two diode-connected transistors ($\mathrm{M_{D1}}, \mathrm{M_{D2}}$) and two differential pairs ($\mathrm{M_1}$-$\mathrm{M_2}$, $\mathrm{M_3}$-$\mathrm{M_4}$). We set the aspect ratios K of these transistors such that

$$K_{D1} > K_{D2},\ K_1 < K_2,\ \text{and}\ K_3 > K_4. \tag{5}$$

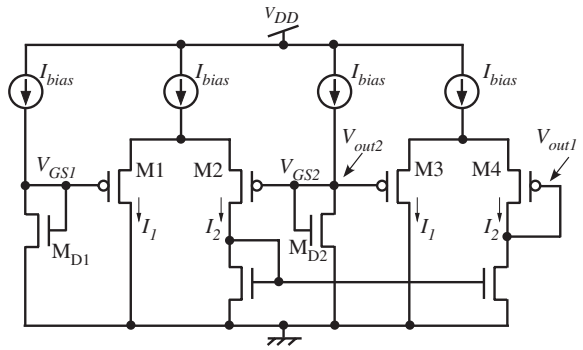

Fig. 1. Floating voltage reference circuit.

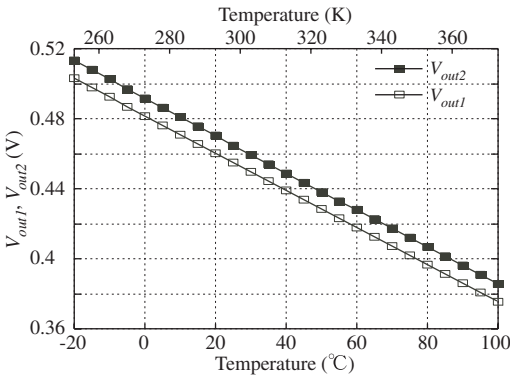

Fig. 2. Simulated output voltages V_{out1} and V_{out2}.

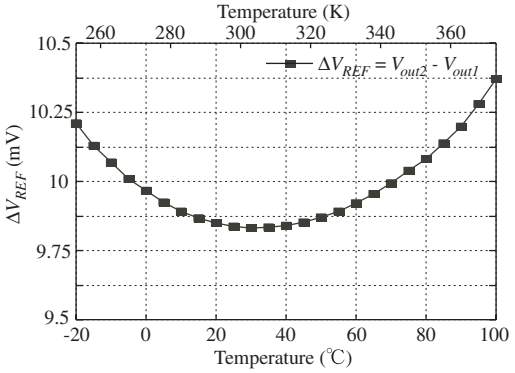

Fig. 3. Floating reference voltage ΔV_{REF}.

The circuit generates output voltages on output terminals (V_{out1}, V_{out2}), and the difference in the voltages is the floating millivolt reference voltage. The floating reference voltage is equal to the sum of the differences in threshold voltage for different transistor size. The threshold voltage of a transistor depends on the length and width of its channels [5]. Therefore, the difference in threshold voltage can be used to generate a floating millivolt reference voltage. Output voltages V_{out1} and V_{out2} have a negative dependence on temperature, whereas the difference in the voltage of $V_{out2}-V_{out1}$ shows a temperature-insensitive constant reference voltage. The details on the circuit operation are as follows.

The diode-connected MOSFETs $\mathrm{M_{D1}}$ and $\mathrm{M_{D2}}$ are operated in the subthreshold region, and their gate-source voltages $V_{GS,D1}$ and $V_{GS,D2}$ are given by

$$V_{GS,Di} = V_{TH,Di} + \eta V_T \ln\left(\frac{I_{bias}}{K_{Di} I_0}\right) \quad (i = 1, 2). \tag{6}$$

The difference in the gate-source voltages $\Delta V_{GS,D}$ in $\mathrm{M_{D1}}$ and $\mathrm{M_{D2}}$ can be expressed as

$$\Delta V_{GS,D} = \Delta V_{TH,D21} + \eta V_T \ln\left(\frac{K_{D1}}{K_{D2}}\right), \tag{7}$$

where $\Delta V_{TH,D21} (= V_{TH,D2} - V_{TH,D1})$ is the difference in the threshold voltages. The resulting currents I_1 and I_2 in differential pair $\mathrm{M_1}$-$\mathrm{M_2}$ are given by

$$I_i = K_i I_0 \exp\left(\frac{V_s - V_{GS,Di} - V_{THi}}{\eta V_T}\right) \quad (i = 1, 2), \tag{8}$$

where V_s is the common-source node voltage of the differential pair. Current I_2 is copied into the $\mathrm{M_4}$ of the differential pair $\mathrm{M_3}$-$\mathrm{M_4}$. Because the currents in transistors $\mathrm{M_3}$ and $\mathrm{M_4}$ are I_1 and I_2, gate-source voltages $V_{GS,3}$ and $V_{GS,4}$ are given by

$$V_{GS,i+2} = V_{TH,i+2} + \eta V_T \ln\left(\frac{I_i}{K_{i+2} I_0}\right) \quad (i = 1, 2). \tag{9}$$

The difference ΔV_{REF} (=$V_{out2}-V_{out1}$) in the output voltages is given by

$$\Delta V_{REF} = V_{GS,4} - V_{GS,3}. \tag{10}$$

Equation (10) can be rewritten from Eqs. (7), (8), and (9) as

$$\begin{aligned} \Delta V_{REF} &= \Delta V_{TH,43} + \Delta V_{TH,12} - \Delta V_{TH,D21} \\ &\quad + \eta V_T \ln\left(\frac{K_3 K_2 K_{D2}}{K_4 K_1 K_{D1}}\right), \end{aligned} \tag{11}$$

where $\Delta V_{TH,43} (= V_{TH,4} - V_{TH,3})$ and $\Delta V_{TH,12} (= V_{TH,1} - V_{TH,2})$ are the differences in the threshold voltages. We set the aspect ratios K, with condition of Eq.(5), such that

$$K_3 K_2 K_{D2} = K_4 K_1 K_{D1}. \tag{12}$$

Then, the difference in voltage is constant with temperature. The floating voltage reference of the circuit is given by

$$\Delta V_{REF} = \Delta V_{TH,43} + \Delta V_{TH,12} - \Delta V_{TH,D21}. \tag{13}$$

We can obtain the floating millivolt reference by adjusting the size of the transistors.

B. Simulation Results

We confirmed the operation of the circuit by SPICE simulation, assuming a set of 0.35-μm 2P4M-standard CMOS parameters and a 1.5-V power supply.

Figure 2 shows simulated output voltages of V_{out1} and V_{out2} as a function of temperature from –20 to 100 ℃. Both the output voltages decrease linearly with temperature and maintain a constant difference in voltage. Figure 3 shows the floating reference voltage ΔV_{REF}. The difference is

almost constant and was about 10 mV. However, the floating reference voltage increases at low- and high-temperatures, and has nonlinear characteristics due to nonlinearity of the diode-connected transistors. The variations in the reference voltage were about ± 2.7 %. This nonlinearity degenerates the precision with which the PTAT current is generated.

IV. Curvature-Correction Techniques

We develop curvature-correction techniques to improve the accuracy of the floating reference voltage. Several curvature-correction techniques have been presented in the literatures [6]-[9]. We use an idea based on the piecewise-linear curvature-correction technique [9]. The details on circuit operation are as follows.

A. Curvature-Correction Architecture

The correction is performed by changing the bias current in diode-connected transistor $\mathrm{M_{D2}}$. The bias current in diode-connected transistor $\mathrm{M_{D2}}$ is increased at low- and high-temperatures by using curvature-correcting current I_{curv}.

The gate-source voltage $V_{GS,D2}$ of transistor $\mathrm{M_{D2}}$ is now given by

$$V_{GS,D2} = V_{TH,D2} + \eta V_T \ln\left(\frac{I_{bias} + I_{curv}}{K_{D2} I_0}\right). \quad (14)$$

The difference $\Delta V_{GS,D}$ in the gate-source voltages in $\mathrm{M_{D1}}$ and $\mathrm{M_{D2}}$ can be expressed as

$$\Delta V_{GS,D} = \Delta V_{TH,D21} + \eta V_T \ln\left(\frac{K_{D1}(I_{bias} + I_{curv})}{K_{D2} I_{bias}}\right). \quad (15)$$

The difference in the output voltage ΔV_{REF} can be given by

$$\begin{aligned}\Delta V_{REF} &= \Delta V_{TH,43} + \Delta V_{TH,12} - \Delta V_{TH,D21} \\ &\quad + \eta V_T \ln\left(\frac{I_{bias}}{I_{bias} + I_{curv}}\right). \end{aligned} \quad (16)$$

Therefore, the curvature-correcting current I_{curv} suppress the increase in the output floating reference at low- and high-temperatures.

B. Circuit for Generating Curvature-Correcting Current

The curvature-correction circuit we developed uses two curvature-correcting currents I_{curv1} and I_{curv2}. We apply the current I_{curv} to node V_{out2} such that

$$I_{curv} = \begin{cases} I_{curv1} & \text{(at low temp.)} \\ 0 & \text{(at middle temp.)} \\ I_{curv2} & \text{(at high temp.)}. \end{cases} \quad (17)$$

The architecture to generate the curvature-correcting current is shown in Fig. 4. We use a PTAT current I_{PTAT} and temperature independent currents I_{REF1}, I_{REF2} to generate the curvature-correcting current. The architecture is based on the nodal subtraction of PTAT current I_{PTAT} and the reference currents of I_{REF1} and I_{REF2}. The reference currents and PTAT current are set so that $I_{REF1} < I_{REF2}$ and that I_{PTAT} has intersecting points with both the reference currents at different temperatures T_1 and T_2 as shown in Fig. 4(a). At

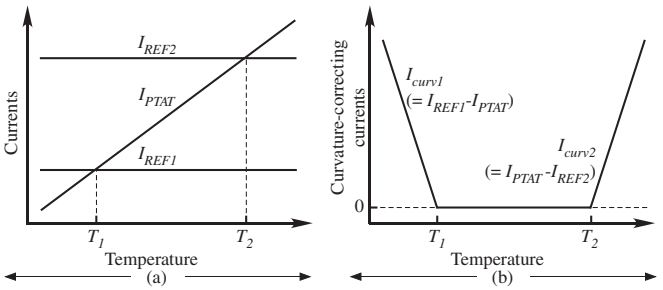

Fig. 4. Architecture for generating curvature-correcting current (I_{curv1}, I_{curv2}) generation.

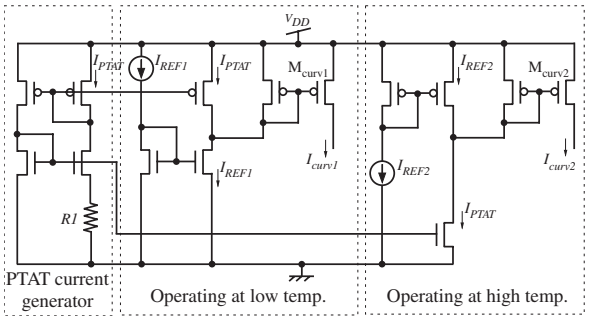

Fig. 5. Circuit for generating curvature-correcting current.

temperatures lower than T_1, $I_{REF1} - I_{PTAT}$ decreases with temperature. At temperatures higher than T_2, $I_{PTAT} - I_{REF2}$ increases with temperature. Figure. 4(b) shows their subtraction currents I_{curv1}, I_{curv2}. From this way, the curvature-correcting current I_{curv} is generated and applied to node V_{out2}. The curvature-correcting current can be summarized as

$$I_{curv} = \begin{cases} I_{REF1} - I_{PTAT} & \text{(at low temp.)} \\ 0 & \text{(at middle temp.)} \\ I_{PTAT} - I_{REF2} & \text{(at high temp.)}. \end{cases} \quad (18)$$

Figure 5 shows the circuit we propose for generating curvature-correcting current, which consists of a PTAT current generator, and two subcircuits that generate curvature-correcting current: one works at low temperature and the other at high temperature.

The PTAT current for the lower temperature range is less than the reference currents: $I_{PTAT} < I_{REF1} < I_{REF2}$, and, therefore, the output transistor $\mathrm{M_{curv1}}$ generates subtracted current $I_{REF1} - I_{PTAT}$. The output transistor $\mathrm{M_{curv2}}$ does not generate any current because transistor $\mathrm{M_{curv2}}$ is in the off state. The PTAT current for a middle temperature range increases more than reference current I_{REF1} and is less than reference current I_{REF2}: $I_{REF1} < I_{PTAT} < I_{REF2}$. The output transistors $\mathrm{M_{curv1}}$ and $\mathrm{M_{curv2}}$ do not generate any currents. The PTAT current for a higher temperature range increases more than the reference currents: $I_{REF1} < I_{REF2} < I_{PTAT}$, and, therefore, the output transistor $\mathrm{M_{curv2}}$ generates subtracted current $I_{PTAT} - I_{REF2}$.

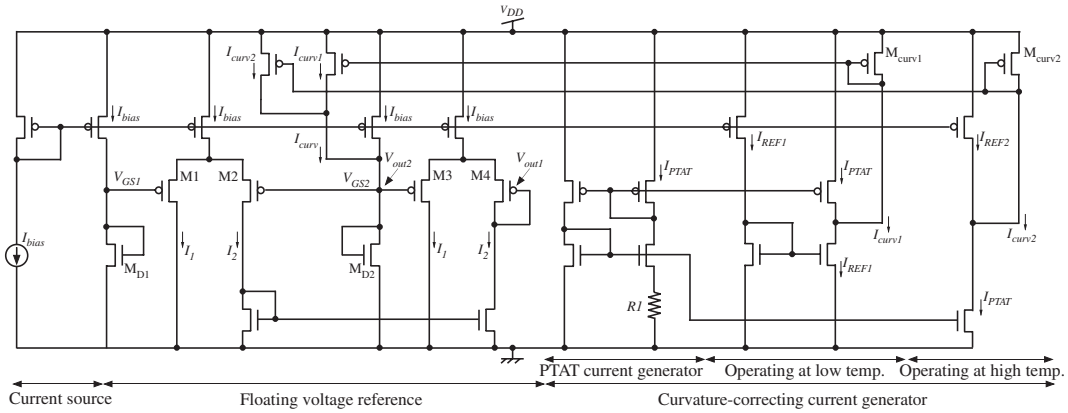

Fig. 6. The floating reference circuit including curvature correction circuit.

C. Simulation Results

We demonstrated the curvature-correction technique by SPICE simulation. Figure 6 shows the entire circuit. The bias current of I_{bias} was set to 100 nA. The reference currents I_{REF1} and I_{REF2} in the curvature-correction circuit were set to 160 nA and 190 nA by changing the current gain factors of the current mirror. Figure 7 shows the simulated curvature-correcting current as a function of temperature. The correcting current I_{curv1} was generated at lower temperature and decreased with temperature. The correcting current I_{curv2} was generated at higher temperature and increased with temperature. These correcting currents were applied to node V_{out2} through the current mirror. Figure 8 shows the output floating reference voltage. The uncorrected reference voltage is also plotted. The variations in the reference voltage were reduced to ± 0.3 % from uncorrected reference variations of ± 2.7 %. The maximum power consumption of the circuit was 4.6 μW at 100 ℃. The floating reference voltage circuit requires a reference current, and the reference circuit in [10] can be used for our purpose.

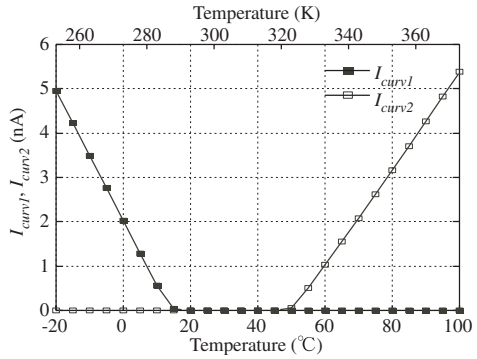

Fig. 7. The simulated curvature-correcting current.

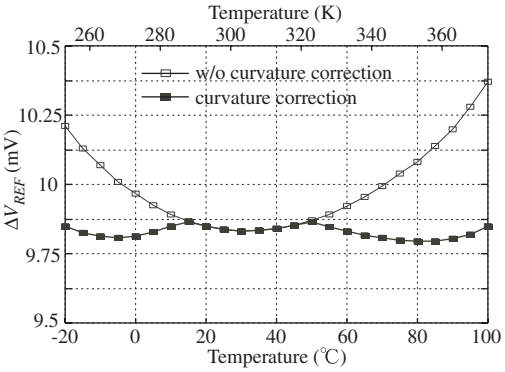

Fig. 8. The output floating reference voltages with and without the curvature correction circuit.

V. Conclusion

We developed a floating millivolt reference circuit to generate PTAT current. The circuit operation was confirmed by simulation with 0.35-μm standard CMOS parameters. The reference voltage was about 10 mV, and the variations were ± 2.7 % in a temperature range from -20 to 100 ℃. The curvature-correction circuit was also developed to improve the accuracy of the reference voltage. The accuracy of the reference circuit could be improved to $\pm$ 0.3 % by using this correction technique. The total power consumption of the circuit was 4.6 μW at 100 ℃.

References

[1] K Ueno, T Hirose, T Asai, Y Amemiya, "Ultralow-power smart temperature sensor with subthreshold CMOS circuits," Proc. International Symposium on Intelligent Signal Processing and Communication Systems, pp. 546-549, Dec. 2006.

[2] Y. Taur, T.H. Ning, "Fundamentals of Modern VLSI Devices," Cambridge University Press, 2002.

[3] P.E. Allen, D.R. Holberg, "CMOS analog circuit design second edition," New York Oxford University Press, 2002.

[4] A.E. Buck, C.L McDonald, S.H Lewis, T.R Viswanathan, "A CMOS bandgap reference without resistors," IEEE J. Solid-State Circuits, vol.37, no.1, pp.81-83, Jan. 2002.

[5] M.C. Hsu, B.J. Sheu, "Inverse-geometry dependence of MOS transistor electrical parameters," IEEE Trans. Computer-Aided Design, vol. CAD-6, pp582-585, July. 1987.

[6] B-S. Song, P.R. Gray, "A precision curvature-compensated CMOS bandgap reference," IEEE J. Solid-State Circuits, vol. SC-18, pp. 634-643, Dec. 1983.

[7] G.C.M. Meijer, P.C. Schmale, K.V. Zalinge, "A new curvature-corrected bandgap reference," IEEE J. Solid-State Circuits, vol. SC-17, pp. 1139-1143, Dec. 1982.

[8] M. Pertijs, K. Makinwa, J. H. Huijsing, "A CMOS smart temperature sensor with a 3σ inaccuracy of ± 0.1℃ from –55℃ to 125℃," IEEE J. Solid-State Circuits, vol. 40, no. 12, pp. 2805-2815, Dec. 2005.

[9] G.A. Rincon-Mora, P.E. Allen, "A 1.1-V current-mode and piecewise-linear curvature-corrected bandgap reference," IEEE J. Solid-State Circuits, vol. 33, pp. 1551-1554, Oct. 1998.

[10] T. Hirose, T. Matsuoka, K. Taniguchi, T. Asai, Y. Amemiya, "Ultralow-power current reference circuit with low temperature dependence," IEICE Trans. Electron., Vol.E88-C, no.6, pp.1142-1147, Nov. 2004.