Low-Power Clock Reference Circuit for Intermittent Operation of Subthreshold LSIs

Ken Ueno, Tetsuya Asai, and Yoshihito Amemiya
Department of Electrical Engineering, Hokkaido University, Sapporo 060-0814 Japan
Tel: +81-11-706-7149, Fax: +81-11-706-7890
E-mail: k_ueno@sapiens-ei.eng.hokudai.ac.jp

***Abstract*— A low power on-chip reference clock generator consisting of subthreshold MOSFET circuits is proposed. It uses a simple frequency-locked loop technique with no inductor, quartz resonator, or MEMS oscillator. Theoretical analyses and a SPICE simulation with 0.35-μm CMOS parameters showed that the clock frequency could be controlled in the frequency range of 10-1000 kHz. When operated at 170 kHz, the generator showed a temperature coefficient of 100 ppm/°C, a line sensitivity of 3%/V, and a power consumption of 20 μW. Our clock generator can be used as a reference clock for intermittent operation in power aware LSIs.**

I. Introduction

In the near future, new social information infrastructures, or "ubiquitous" network systems, with various smart-sensor devices will be developed and deployed all over the world as a part of the information age [1]. Such network systems will require a huge number of sensor LSIs that measure various physical data in our surroundings, that store and process the measured data, and that output the data on demand (see [2] for an example of such sensors). These sensor LSIs have to operate for a long time with limited energy resources such as microbatteries and energy-harvesting power sources [3]. One possible way of developing such sensor LSIs is to make them with CMOS circuits that operate in the subthreshold region of MOSFETs, i.e., a region at which the gate-source voltage of MOSFETs is lower than the threshold voltage [4]-[5].

Figure 1 shows the chip architecture of smart sensor LSIs that we are developing now. The LSI consists of sensors [2], [6], AD/DA converters, digital signal processors, memories, reference circuits [7]-[9], power supply circuits [10], and transceiver circuits. Microwatt operation requires that, (1) all of the circuits in the LSI are operated in the subthreshold region of MOSFETs, and that (2) the main system of the LSI is operated intermittently under the control of an on-chip reference clock circuit. Intermittent operation contributes to a drastic reduction in the power consumption of the LSI.

This paper focuses on a clock reference circuit indispensable for intermittent operation. Many reference clock circuits have been reported recently [11]-[13] but they are unsuitable for use in power aware LSIs because of their large power consumption (several milliwatts or more), large surface area (over 1 mm^2), and use of MEMS technology incompatible with standard CMOS processes. To solve these problems, we developed a reference clock circuit that can be operated with microwatt-level power consumption, integrated in a small chip area (0.05 mm^2), and fabricated using standard CMOS processes. The circuit makes use of a frequency-locked feedback loop and generates a clock frequency that is insensitive to temperature and the supply voltage.

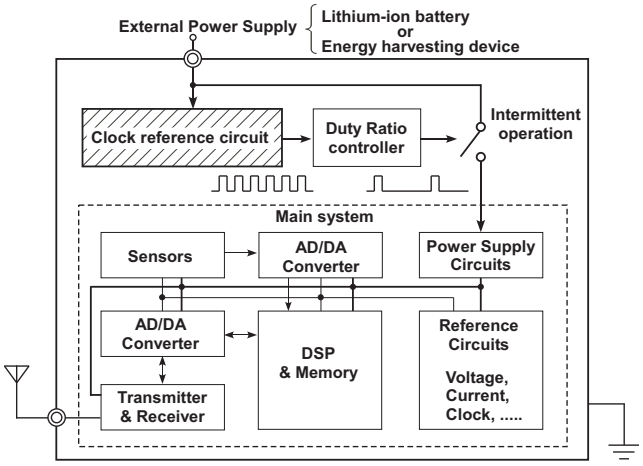

Fig. 1. Chip architecture of microwatt power-aware smart-sensor LSIs.

II. Circuit configuration

Figure 2 shows a block diagram of our reference clock generator. The circuit generates a reference clock using a frequency-locked loop technique. It consists of a current reference, a current comparator, a voltage-controlled oscillator (VCO), and a frequency-to-current converter (see [9] for the current reference circuit), and these circuits form a feedback loop. The current comparator detects the difference between the reference current I_{REF} and the output current I_{OUT} of the frequency-to-current converter and generates the output voltage V_{OUT} proportional to the difference. The VCO accepts the output voltage V_{OUT} and produces oscillation pulses with a frequency f_{REF} dependent on V_{OUT}. The frequency-to-current converter accepts the oscillation pulses and generates the output current I_{OUT} proportional to f_{REF}. Then the current comparator again compares currents I_{REF} and I_{OUT} to produce a readjusted V_{OUT}. This feedback operation is repeated to make I_{OUT} equal to I_{REF}. The resultant clock frequency f_{REF} is independent of temperature and power supply voltage.

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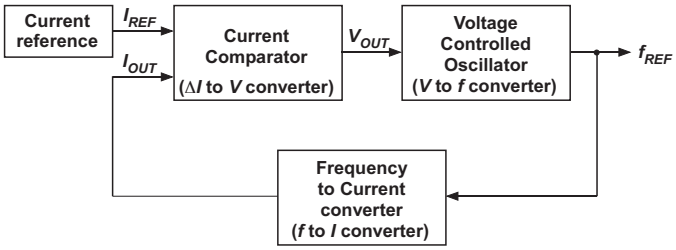

Fig. 2. Block diagram of our reference clock generator.

Figure 3 shows the configuration of our clock generator. All MOSFETs in the circuit are operated in the subthreshold region to achieve ultra-low power consumption. The following sections describe the operation of the generator in detail.

A. Current Comparator (block (B) in Fig. 3)

The current comparator is a common-source circuit used to detect the difference between reference current I_{REF} and output current I_{OUT} of the frequency-to-current converter. It generates output voltage V_{OUT} proportional to the difference between the two. The reference current I_{REF} (about 60 nA) that is independent of the temperature and supply voltage is provided by a subthreshold reference current circuit (not shown in the figure, see [9]).

B. Voltage Controlled Oscillator (block (C))

The VCO consists of a current-starved ring oscillator as shown. The circuit is used for producing oscillation pulses that are dependent on output voltage V_{OUT} of the current comparator. Oscillation frequency f_{REF} depends on applied current I_{bias} and is given by

$$f_{REF} = \frac{I_{bias}}{2mAC_LV_{DD}} = \frac{I_0}{2mAC_LV_{DD}} \exp\left(\frac{V_{DD}-V_{OUT}-V_{TH}}{\eta V_T}\right), \quad (1)$$

where m is the number of inverters in the oscillator, C_L is a load capacitance for each inverter, A is a delay fitting parameter [14], I_0 is a process dependent parameter, V_T is the thermal voltage, V_{TH} is the threshold voltage of MOSFETs, and η is the subthreshold slop factor. Oscillation frequency f depends on V_{OUT}.

C. Frequency to Current converter (block (A))

The frequency-to-current converter is a current-to-voltage converter combined with a switched-capacitor resistor. The circuit is used to produce output current I_{REF} proportional to oscillation frequency f_{REF} of the VCO. The voltage of one end of the switched-capacitor resistor is fixed to reference voltage V_{REF} with an operational amplifier and a MOSFET, where the reference voltage is supplied by a voltage reference circuit consisting of subthreshold MOSFETs (see [7] for this voltage reference). The switched-capacitor resistor consists of capacitor C_S and two switches (sw1, sw2) driven with the oscillation pulses from the VCO, and operates as a resistor

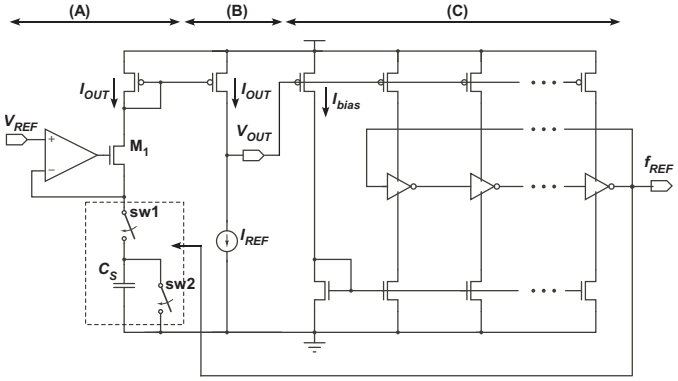

Fig. 3. Schematic of proposed reference clock generator.

with a resistance of $(C_S \cdot f_{REF})^{-1}$. Therefore, output current I_{OUT} of the frequency-to-current converter is

$$I_{OUT} = f_{REF} \cdot C_S \cdot V_{REF}. \quad (2)$$

This current is copied into the current comparator through a current mirror. Because of the feedback operation, the circuit operates so that I_{OUT} will be equal to I_{REF}, and consequently, oscillation frequency f_{REF} will be

$$f_{REF} = \frac{I_{REF}}{C_S \cdot V_{REF}}. \quad (3)$$

Because I_{REF} and V_{REF} are independent of temperature, output frequency f_{REF} is also insensitive to temperature.

This way, a constant reference clock with little dependence on temperature can be obtained.

III. Results

We confirmed the operation of the circuit using a SPICE simulation with a SPECTRE level 53 model and a parameter set of a 0.35-μm 2P4M-standard CMOS process. The supply voltage was set to 3 V (the nominal voltage of lithium-ion batteries). Figure 4 shows the entire construction of our clock reference generator. The VCO consists of seven current-starved inverters connected in a ring. A non-overlapping clock generator was used to prevent switches sw1 and sw2 from being turned on simultaneously. Reference current I_{REF} and reference voltage V_{REF} were set to 60 nA and 0.8 V. Capacitors C_B and C_C remove high frequency noise resulting from the switching operation. The results of the simulation are shown in the following.

The output frequency was adjusted by reference current I_{REF}, and we found oscillation in the 10-1000 kHz frequency range. Figure 5 shows an example with a frequency of 170 kHz. The duty ratio of the waveforms (P) and (Q) as shown in Fig. 4 was about 50%. Figure 6 shows oscillation frequency f_{REF} as a function of temperature from –20 to 80℃with different supply voltages. The variation in frequency was 1.7 kHz, and the temperature coefficient was 100 ppm/℃ for 3-V supply voltage. The circuit operated correctly with a supply voltage higher than 2.2 V. The line sensitivity was 3%/V for a 2.2-3.3 V supply voltage. A constant clock frequency

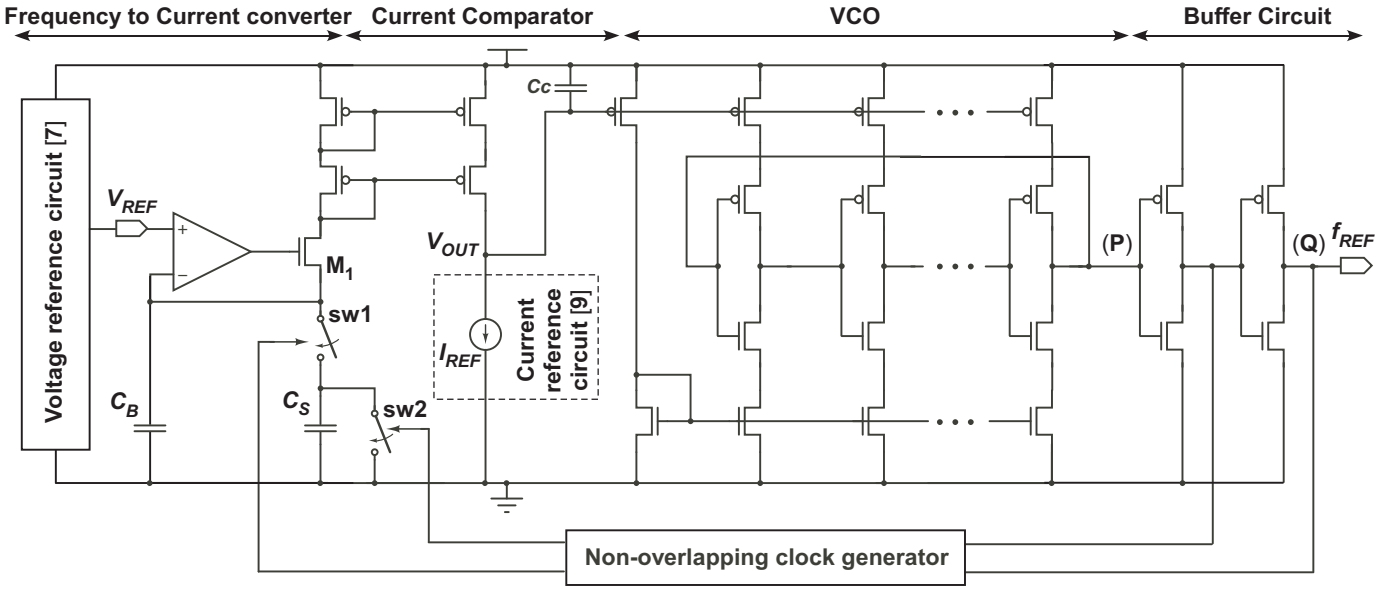

Fig. 4. Entire circuit of reference clock generator. All subcircuits are operated in the subthreshold region except for the buffer circuit and non-overlapping clock generator.

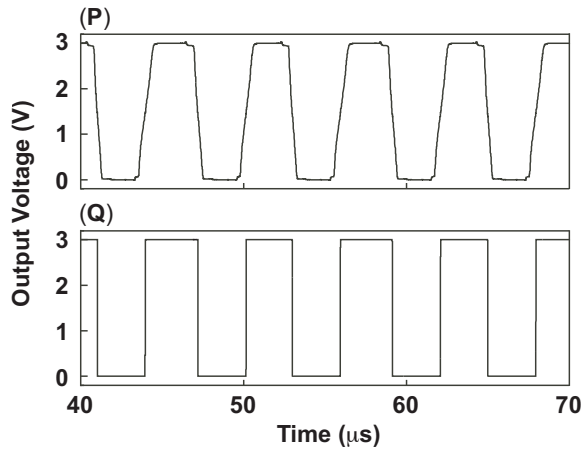

Fig. 5. Output waveform of circuit at room temperature. The duty ratio of the waveform was about 50%.

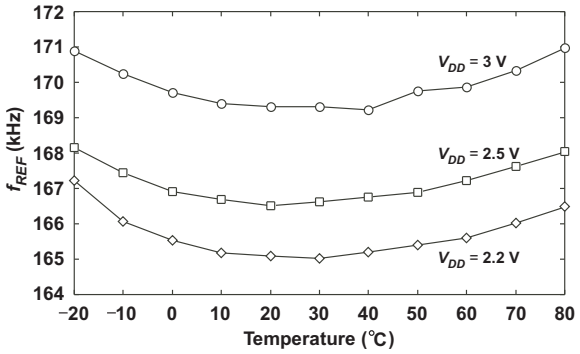

Fig. 6. Oscillation frequency f_{REF} as a function of temperature.

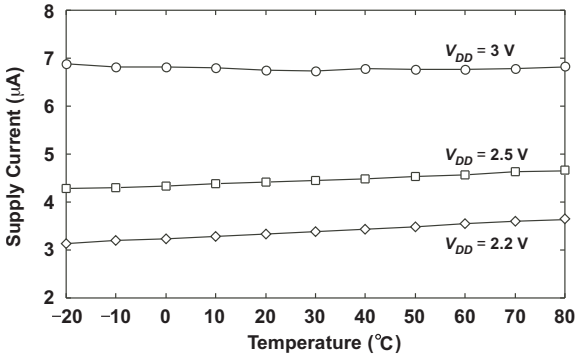

Fig. 7. Supply current as a function of temperature.

that is insensitive to the temperature and power supply was obtained. The lower limit of the supply voltage was reduced to less than 2.2 V using an operational amplifier instead of the cascode current mirrors used in this example. Figure 7 shows the supply current as a function of temperature with supply voltage V_{DD} as a parameter. The supply current with 3-V power supply was about 6.8 μA. The temperature coefficient of the supply current was 0.02%/℃ for V_{DD}= 2.2 V, 0.08%/℃ for 2.5 V, and 0.15%/℃ for 3 V.

To examine the tolerance to device-parameter variation, we performed a corner analysis, using parameters provided by a manufacturer. The worst corners of nMOS and pMOS transistors (S: slow, T: typical, and F: fast) were taken into consideration. Figure 8 shows output frequency f_{REF} for five sets of process corner conditions. The value of f_{REF} changed depending on the set of process corners. This occurred because the reference current I_{REF} and reference voltage V_{REF} depend on process variation. However, the reference clock f_{REF} was independent of temperature in each process corner condition. Figure 9 shows the chip layout of the circuit

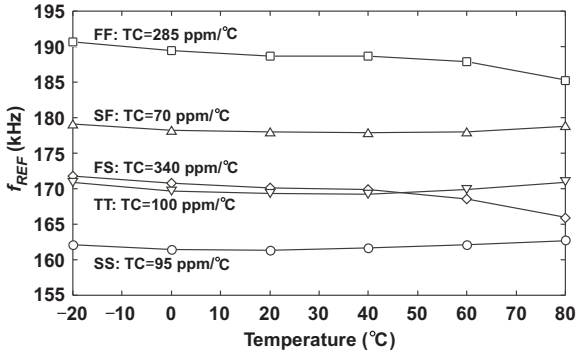

Fig. 8. Output frequency f_{REF} simulated with corner analysis. Process corners of nMOS and pMOS transistors were taken into consideration.

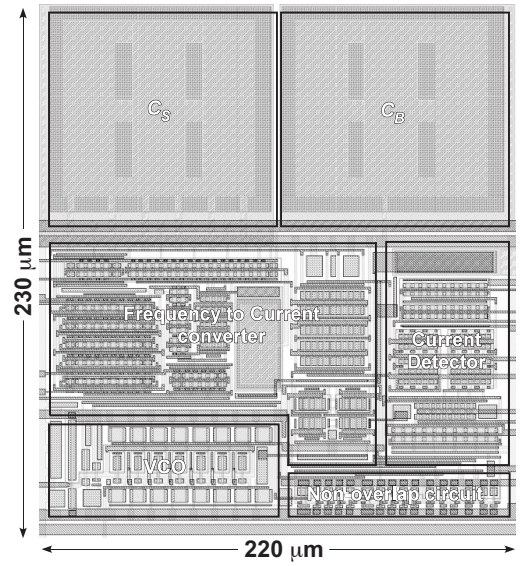

Fig. 9. Layout pattern of reference clock generator (current reference and voltage reference are not shown.)

designed with 0.35-μm, standard CMOS process parameters. The chip area was 0.05 mm^2(=220 μm $\times$ 230 μm), and the power consumption was 20 μW for a 3-V supply voltage. Table I summarizes the performance of our clock generator.

IV. Applications

Our clock generator is compatible with standard CMOS technology and operates with ultra-low power consumption. It can be used as an on-chip timer to control intermittent operation of power aware LSIs as described at the beginning of this paper. The clock generator can also be used as a timer that notifies regular intervals to check and inspect systems. Another possible application is with accumulating sensors. Our clock generator oscillates with a frequency proportional to the reference current, so combining the generator with transducers can construct accumulating sensors that measure the integration of temperature, sunshine, and other environmental parameters. We are now developing various intelligent sensor LSIs that use our on-chip clock generators.

TABLE I
Performance summary

Process	0.35-μm, 2-poly, 4-metal CMOS
Supply voltage	$\geq$ 2.2 V
Temperature range	–20 - 80 ℃
Frequency	170 kHz (@V_{DD} = 3 V)
TC	100 ppm/℃
Line sensitivity	3%/V
Power	20 μW (@V_{DD} = 3 V)
Area	0.05 mm^2

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