On-Chip PVT Compensation Techniques for Low-Voltage CMOS Digital LSIs

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***Abstract*— An on-chip process, supply voltage, and temperature (PVT) compensation technique for a low-voltage CMOS digital circuit is proposed. Because the degradation of circuit performance originates from the variation of the saturation current, a compensation technique that uses a reference current that is independent of PVT variations was developed. The operations of the circuit were confirmed by SPICE simulation with a set of 0.35-μm standard CMOS parameters. Moreover, Monte Carlo simulations assuming process spread and device mismatch in all MOSFETs showed the effectiveness of the proposed technique and achieved performance improvement of 74%. The circuit is useful for on-chip compensation to mitigate the degradation of circuit performance with PVT variation in low-voltage digital circuits.**

I. Introduction

The power dissipation in LSIs has been an important matter in battery-powered electronic devices such as cellular phones, laptops, and portable gadgets. Several techniques to achieve low-power LSI systems have been investigated. Among such techniques, reduction of power supply voltage V_{DD} is the most effective and direct way because power dissipation has a quadratic dependence on supply voltage. Moreover, with recent progress in device technology, the high V_{th} MOSFET–which can further reduce power dissipation–has become available. However, when the values of supply voltage V_{DD} and threshold voltage V_{th} of MOSFETs come close, the variation of threshold voltage has a significant impact on circuit performance. This is because the saturation current of a MOSFET depends on both supply voltage V_{DD} and threshold voltage V_{th}, and the variation of the current can be modeled as $\alpha/(V_{DD}-V_{th})$ [1]. Both low supply voltage operation and the use of high V_{th} MOSFET therefore tend to increase variation in circuit performance.

The variation of threshold voltage in a MOSFET is due to process and temperature variations, namely, about $\pm$0.1 V and 0.1 V (in a temperature range of –20℃ to 100℃), respectively. The variation degrades circuit performance; accordingly, LSI designers should pay much attention to the variations. Several compensation techniques have been reported [2]-[6]. In [2] and [3], a reference clock was used to compensate the variation, and in [4]-[6], a substrate biasing or supply voltage control, or both, were used. However, these techniques consist of several circuit blocks and then become a complex circuit configuration. Moreover, the accuracy of the compensation techniques becomes worse at higher temperature.

To solve these problems, in this study, we developed an on-chip process, supply voltage, and temperature (PVT) compensation techniques for low-voltage CMOS digital circuits. Because the degradation in performance of the circuit comes from the variation of saturation current due to variation of threshold voltage under low-voltage operation, a compensation technique using a reference current that is independent of PVT variations was developed. The circuit has a compact configuration and is useful for low-voltage CMOS digital LSI systems.

II. Effect of process variations in LSIs

The variation of threshold voltage can be classified broadly into two categories [7], [8]: within-die (WID), or intra-die, variation and die-to-die (D2D), or inter-die, variation. The former affects the relative accuracy of transistors placed closely within a chip and depends on the transistor sizes [9]. The latter affects the absolute accuracy of the chip and degrades the performance between chips. Because digital circuits consist of minimum-sized transistors, the performance of digital circuits is affected by both WID and D2D variations. However, according to central limit theorem, the effect of WID variations is statistically averaged out to the value defined by the D2D variations [8]. Because digital circuits are used in a cascade, the effect of WID variations will be small. However, the D2D variations cannot be ignored.

In the present study, to evaluate the effects of process variations in digital circuits, a delay variation of a CMOS inverter chain was analyzed. Monte Carlo simulations assuming D2D variations (the parameters were varied with a uniform distribution, e.g., –0.1 V $< \delta V_{th} <$ 0.1 V) and WID mismatch variations (the parameters were varied a Gaussian distribution, e.g., $\sigma_{V_{th}} = A_{V_{th}}/\sqrt{LW}$) in all MOSFETs were performed by using the parameters provided by the manufacturer.

A. Delay Analysis

The delay τ of an inverter can be expressed by

$$\tau = \frac{C_{load} V_{DD}}{I_{on}}, \tag{1}$$

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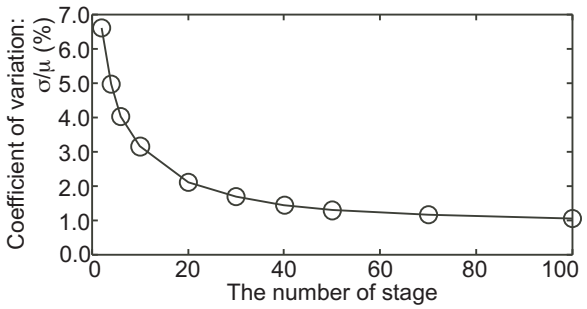

Fig. 1. Delay variation of an inverter as a function of the number of inverter stages from 100-runs Monte Carlo simulations assuming WID variations. Supply voltage: 1 V.

where C_{load} is load capacitance, V_{DD} is supply voltage, and I_{on} is saturation current. Saturation current I_{on} is given by

$$I_{on} \sim \frac{W}{L}\mu C_{ox}\left(V_{DD}-V_{th}\right)^{\alpha}, \tag{2}$$

where L is channel length, W is channel width, μ is carrier mobility, C_{ox} is gate oxide capacitance, and α is a carrier mobility degradation factor [10]. Load capacitance C_{load} can be approximated by the gate capacitance of the next inverter stage and is given by $C_{load} \sim C_{ox}LW$. Under the assumption that each parameter in Eqs. (1) and (2) varies $\pm\delta$ from the typical value, the delay variation $\delta\tau/\tau$ is expressed as

$$\frac{\delta\tau}{\tau} \sim f\left(2\frac{\delta L}{L}, \frac{\delta\mu}{\mu}, \frac{\alpha}{V_{DD}-V_{th}}\delta V_{th}\right), \tag{3}$$

where f is the characteristic function derived from Eqs. (1) and (2). Delay variation $\delta\tau/\tau$ depends on terms of channel length variation $\delta L/L$, carrier mobility variation $\delta\mu/\mu$, and threshold voltage variation $\delta V_{th}/(V_{DD}-V_{th})$, which depends on supply voltage. In general, the degradation in performance of a digital circuit is dominated by the channel length variation. However, in low-voltage digital circuits, threshold voltage variation becomes a key factor in the delay variation $\delta\tau/\tau$ instead of the channel length variation.

B. Impact of WID Variations

To study the effect of WID variation on circuit performance, an inverter chain circuit was analyzed by Monte Carlo simulation considering WID variations. Because the delay has a Gaussian distribution (σ: standard deviation, μ: average), the coefficient of variation (σ/μ) of the delay per inverter stage was evaluated. Figure 1 plots the coefficient of variation as a function of the number of inverter stages. Clearly, (σ/μ) decreases as the number of inverter stages increases. This is because WID variations of an inverter are averaged as the number of inverter stages increases. In most digital circuits, the number of stages is high enough, so the effect of WID variations is small compared to the D2D variations.

C. Impact of D2D Variations

To verify the effect of the D2D process variations, Eq. (3) was solved numerically with parameters for a 0.35-μm CMOS. Because the threshold voltage of a pMOSFET (0.72 V) is 1.4 times larger than that of an nMOSFET (0.52 V) in the process we used, the variation of threshold voltage of the pMOSFET has a significant impact on circuit performance. Figure 2 plots the calculated delay variation ($\delta\tau/\tau$) of an inverter as a function of D2D pMOSFET threshold voltage variation δV_{thp} and D2D channel length variation δL. For a supply voltage of 2 V (Fig. 2(b)), the impacts of pMOSFET threshold voltage variation and channel length variation are comparable. However, at a lower voltage of 1 V (Fig. 2(a)), the delay variation with pMOSFET threshold voltage variation δV_{thp} increases drastically. The delay variations of the circuit were analyzed by SPICE simulation with Monte Carlo analysis assuming D2D variations. Figure 3 shows simulated delay variation of an inverter as a function of supply voltage. The results in the case that parameters V_{thn}, V_{thp}, and L were varied individually are also plotted in order to separate the effect of each parameter on the delay variation. At higher voltage ($V_{DD} > 1.2$ V), the delay variation was dominated by the channel length variation. On the other hand, at lower voltage ($V_{DD} < 1.2$ V), the effect of the pMOSFET threshold voltage variation got worse than that of channel length variation and became a key factor of the delay variation. Therefore, the variation of threshold voltage has a significant impact on digital circuit performances at a low voltage operation.

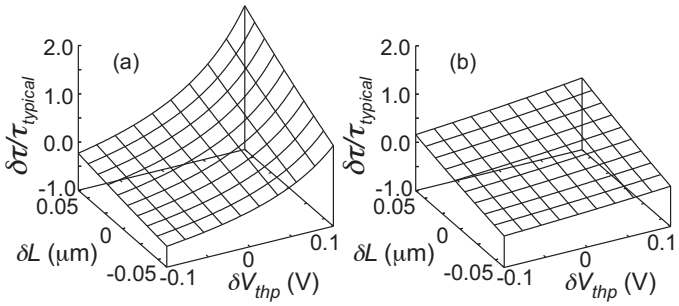

Fig. 2. Calculated delay variation of an inverter as a function of pMOSFET threshold voltage variation δV_{thp} and channel length variation δL. (a) Supply voltage: 1 V; (b) supply voltage: 2 V.

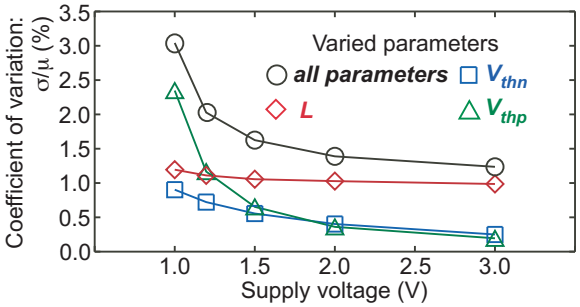

Fig. 3. Delay variation of inverter as a function of the supply voltage from 100-runs Monte Carlo simulations assuming D2D variations. The results that parameters varied individually are also plotted.

III. Temperature Variation

Temperature variation also causes performance degradation in CMOS digital LSIs because parameters such as threshold voltage V_{th} and mobility μ depend on temperature. In this section, the temperature dependence of the low-voltage digital circuit is discussed.

The temperature dependence of threshold voltage V_{th} and

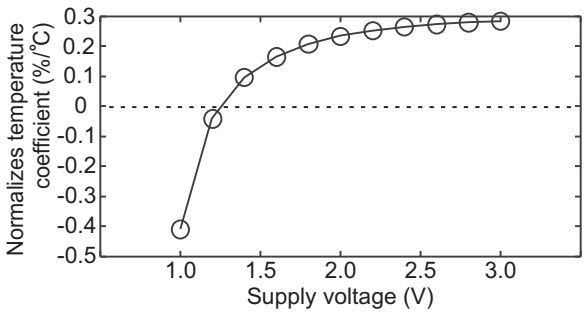

Fig. 4. Simulated normalized temperature coefficient of inverter delay as a function of supply voltage.

mobility μ is given by

$$\mu = \mu_0 \left(\frac{T_0 + \delta T}{T_0} \right)^{-m}, \quad V_{th} = V_{th0} - \kappa \left(T_0 + \delta T \right), \quad (4)$$

where μ_0 is carrier mobility at room temperature, m is the mobility temperature exponent, T_0 is room temperature, δT is the temperature change from T_0, V_{th0} is the threshold voltage at absolute zero temperature, and κ is the temperature coefficient of the threshold voltage [11].

From Eqs. (1), (2), and (4), the delay variation $\delta\tau/\tau$ with temperature is given by

$$\frac{\delta\tau}{\tau} \sim \left(\frac{m}{T_0} - \frac{\alpha\kappa}{V_{DD} - V_{th0} + \kappa T_0} \right) \delta T. \quad (5)$$

As with the process variation discussed in the previous section, the variation of delay with temperature depends on supply voltage, as shown in the second term of Eq. (5).

Figure 4 shows the simulated temperature coefficient of the delay in an inverter as a function of supply voltage. The temperature coefficient is positive at a higher supply voltage because the second term in Eq. (5), which depends on supply voltage and threshold voltage, has quite little dependence on the delay variation at the voltage region. It is thus concluded that the temperature dependence of carrier mobility is a key factor in the variation of delay. However, at lower voltage, the temperature coefficient gradually decreases with decreasing supply voltage as a result of the second term in Eq. (5). At a supply voltage of 1.1 V, the temperature coefficient of the circuit becomes zero. This result means that the first and second terms in Eq. (5) became comparable at supply voltage. At a supply voltage below 1.1 V, the temperature coefficient becomes negative, and the second term in Eq. (5) becomes a key factor in the variation of delay.

IV. Compensation technique

As explained in previous sections, the delay variation of the circuit depends on both supply voltage V_{DD} and threshold voltage V_{th} when the circuit operates at low supply voltage. To operate the circuit at low supply voltage while sufficient performance is maintained, a compensation technique is required. Accordingly, as explained in this section, an on-chip process compensation technique for low-voltage digital circuits–which uses a reference current that is tolerant to PVT variations–was devised.

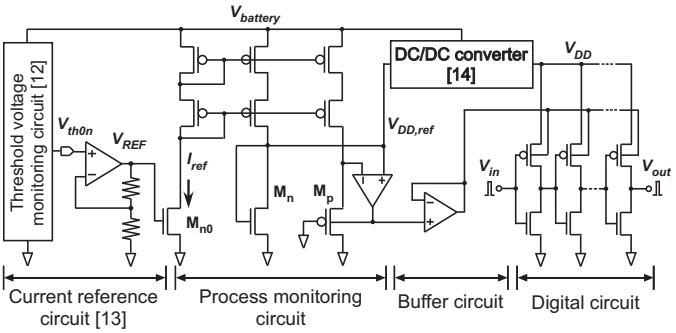

Fig. 5. Schematic of proposed compensation circuit.

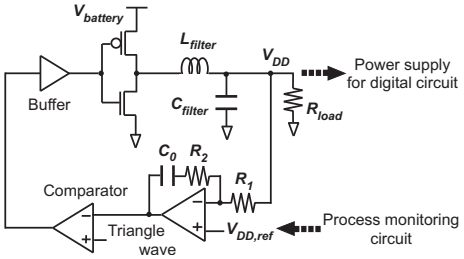

Fig. 6. Schematic of DC/DC converter based on PWM control [14].

A. Circuit Configuration & Operation Principle

The developed compensation technique uses a reference current I_{ref} that is independent of PVT variations. The reference current I_{ref} is generated by a threshold voltage monitoring circuit [12], a non-inverting amplifier, and an output transistor M_{n0}. (The circuit configuration is shown on the left hand side of Fig. 5.) The threshold voltage monitoring circuit generates a voltage V_{th0n} that is based on the threshold voltage of a MOSFET at absolute zero temperature [12]. Output voltage V_{th0n} has linear dependence on D2D threshold voltage variation. Therefore, by making use of the voltage as a bias voltage for a transistor, a reference current that is independent of threshold voltage variation can be obtained because the output voltage monitors the threshold voltage in an LSI chip. However, although the variation of threshold voltage can be canceled by the monitoring circuit, temperature dependence of the mobility still exists. To compensate for the temperature dependence of the current, a non-inverting amplifier is used to cancel the temperature dependence of the mobility. The amplifier accepts and amplifies voltage V_{th0n} to a higher voltage, V_{REF}, by setting the appropriate ratio of resistors so that the temperature coefficient of the current becomes zero. Transistor M_{n0} accepts the voltage V_{REF} and generates a process and temperature compensated reference current I_{ref}. In this way, a reference current that is tolerant to PVT variations can be obtained. The details of the current reference circuit are presented in [13].

Figure 5 shows the entire compensation circuit. The circuit consists of the threshold voltage monitoring circuit, a non-inverting amplifier, a process monitoring circuit, a DC/DC converter, and a buffer circuit. Transistors M_n and M_p are the replica transistors of a digital circuit for monitoring and controlling the process variation. The diode-connected transistor M_n accepts I_{ref} through a pMOS current mirror and generates

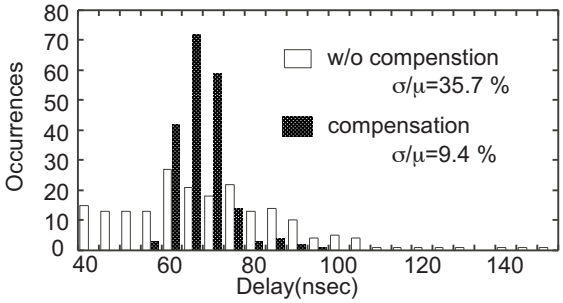

Fig. 7. Distribution of delay in an 100-stage inverter chain with or without a compensation circuit calculated from 200-run Monte Carlo simulations assuming both D2D and WID variations.

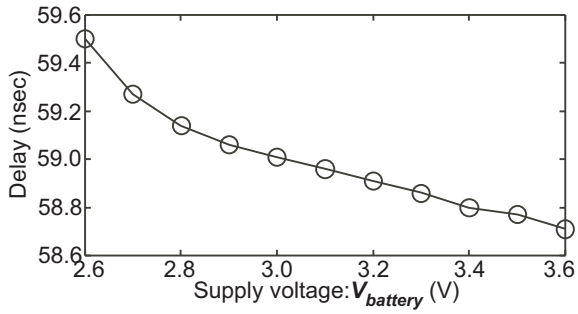

Fig. 8. Simulated delay in 100-stage inverter chain as a function of power supply $V_{battery}$ with compensation circuit.

gate-source voltage $V_{DD,ref}$, which is used as supply voltage V_{DD} for a digital circuit through the DC/DC converter shown in Fig. 6 [14]. Because the supply voltage of nMOSFETs in digital circuits is the same as the replica transistor M_n, the saturation current of nMOSFETs in digital circuits is maintained at the reference current I_{ref}. To control the saturation current of the pMOSFET, a diode-connected transistor M_p, and operational amplifier are used. The operational amplifier monitors the gate-source voltages of transistors M_n and M_p through the bulk terminal of transistor M_p. The operational amplifier operates so that the gate-source voltage of M_p is equal to that of M_n. And the voltage of the bulk terminal of transistor M_p is controlled so that the current of pMOSFET in digital circuits is equal to the reference current I_{ref}. The buffer circuit accepts the generated bulk voltage and applies it to the bulk terminals of the pMOSFETs in digital circuits in order to control the saturation current in the pMOSFETs. This way the saturation current in both the nMOSFETs and pMOSFETs in the digital circuits are kept to reference current I_{ref}. Because reference current I_{ref} is independent from D2D process and temperature variation, PVT variations of the digital circuits can be compensated.

B. Simulation Results

The operations of the circuit were confirmed by Monte Carlo simulations assuming both D2D and WID variations. Voltage $V_{battery}$ was set to 3.3 V (under the assumption that a lithium-ion rechargeable battery is used). The delay variation of a 100-stage inverter chain was studied by setting supply voltage V_{DD} at 1 V. Figure 7 shows the distribution of the delay variation of the circuit. The process sensitivities (σ/μ) in the case with or without the compensation technique

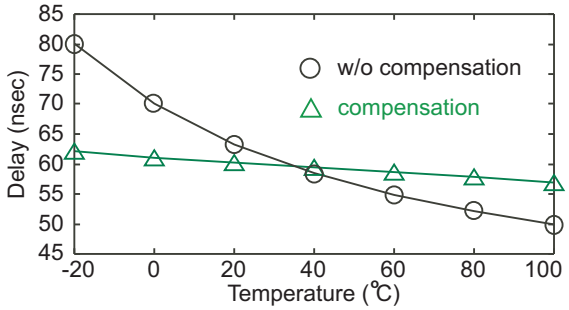

Fig. 9. Simulated delay in 100-stage inverter chain as a function of temperature in case with or without compensation circuit.

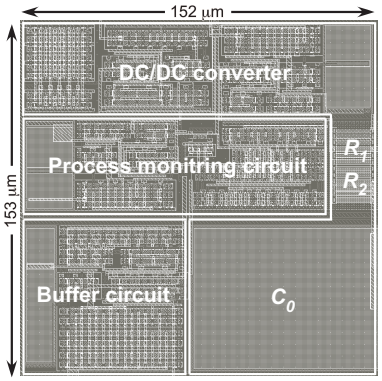

Fig. 10. Layout pattern of proposed circuit. Its area is 0.023 mm^2

were 9.4% and 35.7%, respectively, and can be improved to about 74% by using the proposed compensation technique. Figure 8 shows the simulated delay of a 100-stage inverter chain with the compensation circuit as a function of voltage $V_{battery}$. The dependence of $V_{battery}$ is quite small (i.e., within 1.0%). The line regulation of the delay is 1.3%/V. Figure 9 shows the simulated delay as a function of temperature from –20℃ to 80℃. In the with-compensation case, delay is almost constant with little temperature dependence. The temperature dependence was 0.07%/℃. Figure 10 shows a layout pattern of the proposed circuit. The area including DC/DC converter is 0.023 mm^2.

In a battery-powered system, a DC/DC converter is required to convert a battery voltage to a lower voltage for LSIs. The proposed technique is useful for on-chip process, supply voltage, and temperature compensation of digital circuits in combination with a DC/DC converter.

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