Power Supply Circuits for Ultralow-Power Subthreshold CMOS Smart Sensor LSIs

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***Abstract*— A low-voltage power supply circuit was developed for micropower CMOS LSI applications, with microwatt smart-sensor LSIs being the specific focus. The circuit consists of a switched-capacitor voltage converter and a series regulator. The switched converter lowers battery voltage by 1.5–3 V to a low voltage of 0.5–0.7 V that drives the series regulator, and the series regulator provides LSI logic gates with a power voltage of 0.4–0.6 V such that the logic gates operate at a subthreshold region. The switched converter lowered the voltage of a 1.5-V battery to 0.68 V in a sample circuit designed to produce a supply voltage of 0.6 V, and the series regulator lowered it further to 0.6 V. The power efficiency of the switched converter is 83 %, and the total efficiency is 73 % with a 13-μA output current.**

I. Introduction

New social information infrastructures, or "ubiquitous" network systems, will be developed to provide promising communication platforms for collecting and delivering information throughout the world. Such systems need a tremendous number of distributed smart sensor LSIs to measure various physical data in our surroundings, store and process the measured data, and output the data on demand (see [1], [2] for an example of such sensors). These sensing LSIs must operate with ultralow power, e.g., a few microwatts or less, because they will probably be placed under conditions where they have to get their necessary energy from microbatteries or from less-than-ideal surroundings such as ones with poor sunlight, weak electric waves, and slight differences in daytime and nighttime temperatures.

Figure 1 depicts the architecture of such smart sensor LSIs. An LSI consists of sensors, AD/DA converters, digital signal processors, memories, reference circuits, and power supply circuits. To achieve microwatt operation, all of the circuits in the LSI have to be operated in the subthreshold region of MOSFETs, i.e., a region at which the gate-source voltage of MOSFETs is lower than the threshold voltage.

For the subthreshold operation of processors and memories, CMOS digital gates have to be operated under a low power voltage of about 0.4–0.6 V. However, the external supply voltage available is far higher than the desired values: for example, the supply voltage is 1.5 V in manganese batteries and 3 V in lithium batteries. Therefore, an on-chip DC–DC converter is required to lower the battery voltage to 0.4–0.6 V with high efficiency. Although various DC–DC converters have been developed [3]–[6], all of them are designed for high-power applications and operate efficiently only at milliwatt or larger power operation. Therefore, ordinary DC–DC converters are unsuitable for our purpose, i.e., microwatt or less power applications.

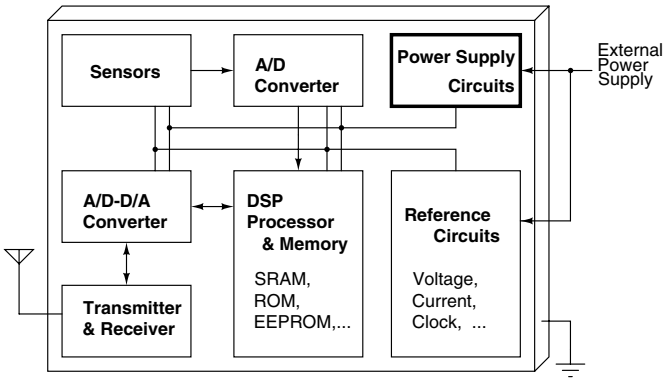

Fig. 1. Chip architecture of microwatt smart-sensor LSIs.

To overcome this problem, we developed a power-supply circuit consisting of a low-voltage DC–DC converter and a series regulator specialized for microwatt operation. This paper describes a design method for an efficient microwatt DC–DC converter with control circuits for subthreshold LSI applications.

II. Switched Capacitor DC–DC Converter

A. Step-down SC DC–DC Converter

Figure 2 shows the SC voltage divider. The circuit consists of two capacitors (C_1 and C_2) and four switches. The capacitors are connected in series and in parallel periodically with a two-phase switching clock so that the circuit generates half of the input voltage. The voltage of C_2 in parallel connection, V_{2n}, with the charge conservation law of the capacitors can be given by

$$V_{2n} = \left(\frac{C_1 - C_2}{C_1 + C_2}\right)^{2n} \left(V_{2,0} - \frac{1}{2}V_{IN}\right) + \frac{1}{2}V_{IN} \quad , \qquad (1)$$

where n is the number of the switching cycle, and $V_{2,0}$ is the initial voltage of capacitor C_2 (see [7]). Because the geometric ratio in Eq. (1) is less than 1, voltage V_{2n} converges to half of the input voltage after sufficient switching cycles:

$$V_{2n}|_{2n\to\infty} \to \frac{1}{2}V_{IN} \quad . \qquad (2)$$

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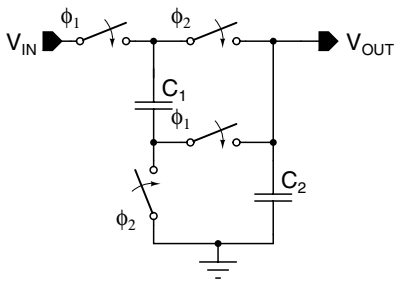

Fig. 2. Schematic of step-down SC DC–DC voltage converter.

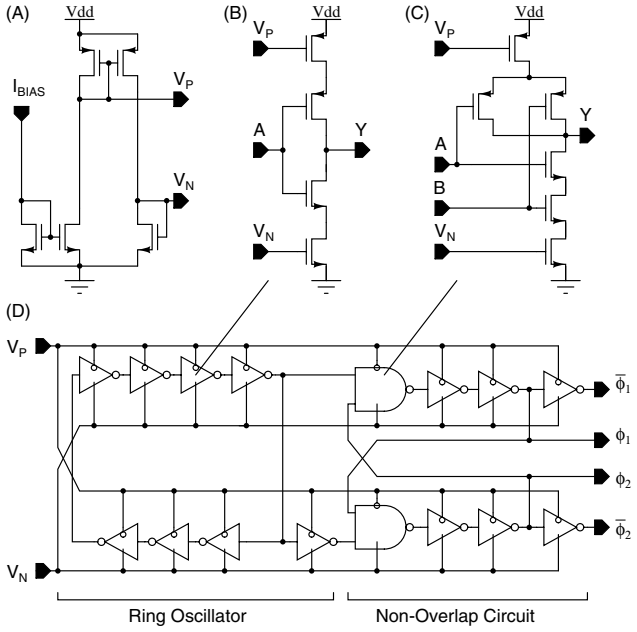

Fig. 3. Schematics of (A) bias generation circuit, current starved (B) inverter and (C) NAND gate, and (D) ring oscillator and nonoverlapping clock generation circuit.

Therefore, the circuit in Fig. 2 generates half of the input voltage without any dependence on the initial voltage, size and ratio of the capacitors.

B. Clock Generation Circuit

The SC DC–DC voltage converter in Fig.2 generates half of the input voltage by using a two-phase switching clock. The clock generation circuit, which consists of ordinary inverters and NAND gates, could not be used in our converters because of the short current of the CMOS logic gates. Current starved inverters and NAND gates are used to reduce the power consumption in our clock generation circuit.

Figure 3(A) shows the bias voltage generation circuit for the current control of the digital gates. The voltage V_P and V_N are generated by an nMOSFET and pMOSFET current mirror configuration with reference current I_{REF}. Figure 3(B) and (C) show the current starved inverter and NAND gate, respectively. The short current of the circuit is controlled by the voltage V_P and V_N. Figure 3 (D) shows the clock generation

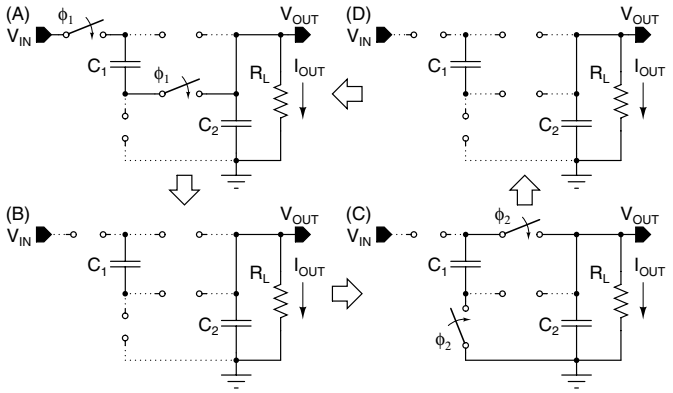

Fig. 4. Four-state connection of SC DC–DC converter.

circuit we use. The circuit consists of a ring oscillator and nonoverlapping clock generation circuit. Because the short current of the inverter is controlled by voltage V_P and V_N, the output waveform of the circuit increases and decreases gradually. Although the oscillation frequency is quite low because of the large inverter's delay, no interference occurs in the converter operation. A nonoverlapping clock generation circuit is used to ensure that both switches for the series and parallel connection should turn on separately because the SC DC–DC converter uses a two-phase clock.

C. Converter Operation with a Load

The charge in the capacitor is discharged to a load as an output current, and the output voltage decreases as the output current increases. Moreover, the period when all switches turn off occurs at the same level as the "on" states due to the low oscillation frequency and the slow propagation time in the clock generation circuit. Because turning "off" the timing of the switches could not be neglected, the output voltage decreases considerably when all of the switches are turned off. Therefore, the SC DC–DC converter operates in a four-state connection. These four states are shown in Fig.4. By switching clock ϕ_1, the capacitors are connected in series (state (A)), and then all the switches turn off (state (B)). After that, by switching clock ϕ_2, the capacitors are connected in parallel (state (C)), and then all the switches turn off (state (D)). The converter generates output voltage V_{OUT} by repeating these four states. For the sake of simplicity, we performed the circuit analyses under conditions where all the capacitances were the same size $C_{1,2} = C$, the switch resistance was R, and the load resistance was R_L.

In series and parallel connections (state (A) and (C)), the circuit equation is given in the form of a second order differential equation and can be expressed as

$$\frac{d^2Q_2}{dt^2} + \frac{R_L + R}{R_L RC}\frac{dQ_2}{dt} + \frac{Q_2}{2R_L RC^2} = 0 \quad , \qquad (3)$$

where Q_2 is the charge in capacitor C_2. In a condition where load resistance, R_L, is sufficiently larger than switch resistance, R, or $R_L \gg R$, Eq. (3) can be solved analytically.

In the series connection (state(A)), the charge $Q_{2,A}$ can be given by

$$Q_{2,A} = \alpha_A \exp\left(-\frac{t}{RC}\right) + \beta_A \exp\left(-\frac{t}{2R_LC}\right) \quad , \quad (4)$$

$$\alpha_A = -\frac{R_L(CV_{IN} - Q) - RQ_{20,D}}{2R_L - R} \quad , \quad (5)$$

$$\beta_A = \frac{2(R_L - R)Q_{20,D} + R_L(CV_{IN} - Q)}{2R_L - R} \quad , \quad (6)$$

$$Q = Q_{10,D} + Q_{20,D} \quad , \quad (7)$$

where $Q_{10,D}$ and $Q_{20,D}$ are the charges of C_1 and C_2 at the end of state (D), respectively. Because α_A is negative and β_A positive, the charge Q_2, which is the voltage of V_{OUT} (=Q_2/C_2), increases with time constant RC and then decreases with time constant $2R_LC$. In a similar way, the charge $Q_{2,C}$ in the parallel connection (state (C)) can be given by

$$Q_{2,C} = \alpha_C \exp\left(-\frac{t}{RC}\right) + \beta_C \exp\left(-\frac{t}{2R_LC}\right) \quad , \quad (8)$$

$$\alpha_C = -\frac{R_L\Delta Q - RQ_{20,B}}{2R_L - R} \quad , \quad (9)$$

$$\beta_C = \frac{2(R_L - R)Q_{20,B} + R_L\Delta Q}{2R_L - R} \quad , \quad (10)$$

$$\Delta Q = Q_{10,B} - Q_{20,B} \quad , \quad (11)$$

where $Q_{10,B}$ and $Q_{20,B}$ are the charges of C_1, and C_2 at the end of state (B), respectively. Just as with the series connection, because α_C is a negative value and because β_C is a positive value, the voltage of V_{OUT} increases with time constant RC and then decreases with time constant $2R_LC$.

The circuit equation is given in the form of a differential equation for when all switches are turned off (state (B) and (D)) and can be expressed as,

$$\frac{dQ_2}{dt} + \frac{Q_2}{R_LC} = 0 \quad . \quad (12)$$

Therefore, the charge $Q_{2,i}$ can be expressed as,

$$Q_{2,i} = Q_{20,j} \exp\left(-\frac{t}{R_LC}\right) \quad j = A \text{ or } C \quad , \quad (13)$$

where $Q_{20,A}$ and $Q_{20,C}$ are the charge of C_2 at the end of state (A) and (C), respectively. Therefore, the voltage V_{OUT} decreases with time constant R_LC.

From these analyses, we found that output voltage V_{OUT} increases with time constant RC and decreases with time constant $2R_LC$ in state (A) and (C) and that V_{OUT} decreases with time constant R_LC in state (B) and (D). Therefore, the switching frequency should be an order of time constant RC to achieve a higher power conversion efficiency η (= P_{OUT}/P_{IN}).

III. Circuit Implementation and Operation

The configuration of our power-supply circuit is depicted in Fig.5. The circuits consist of a SC converter and a series regulator. The SC converter lowers external battery voltage V_{IN} to an intermediate low voltage V_{LL}. The series regulator accepts V_{LL} and produces an appropriate supply voltage V_{OUT} such that connected LSI logic gates operate in a subthreshold region.

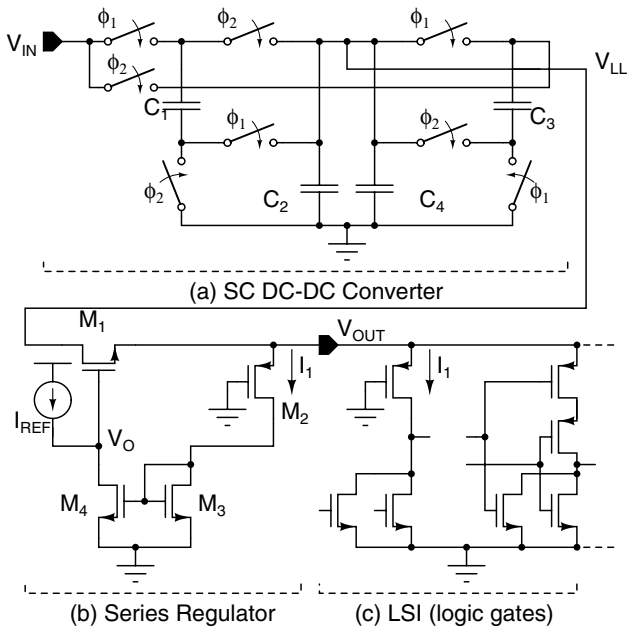

Fig. 5. Power-supply circuits: (a) SC converter, (b) series regulator, and (c) examples of logic gates (NOR).

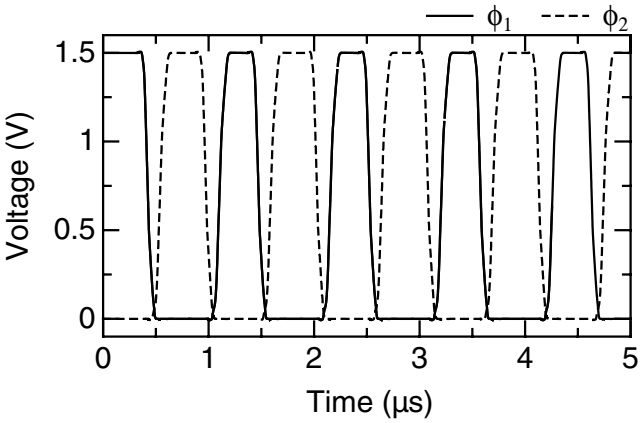

Fig. 6. Characteristics of clock waveforms ϕ_1 and ϕ_2.

In our circuit, we added a complementary divider (capacitors C_3 and C_4 and four more switches) to achieve a high conversion efficiency in low-current, microwatt operation. The divider is driven complementary with clocks ϕ_1 and ϕ_2. The series regulator is controlled by reference current I_{REF} to produce output voltage V_{OUT} such that current I_1 in a monitoring transistor M_2 is equal to I_{REF}. This is performed through negative feedback; $V_{OUT} \rightarrow I_1 \rightarrow$ current in M_4 $\rightarrow V_O \rightarrow$ resistance of $M_1 \rightarrow V_{OUT}$. With this regulation, the supply current through each LSI gate is limited to I_{REF}.

We designed a sample circuit, assumed a set of 0.35-μm standard CMOS parameters and a 1.5-V battery voltage, and

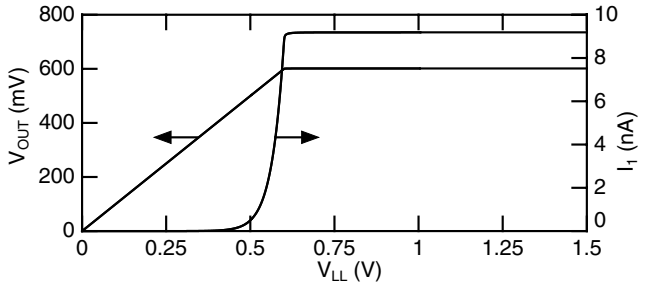

Fig. 7. Characteristics of series regulator: output voltage V_{OUT} and monitored current I_1 as a function of input V_{LL}.

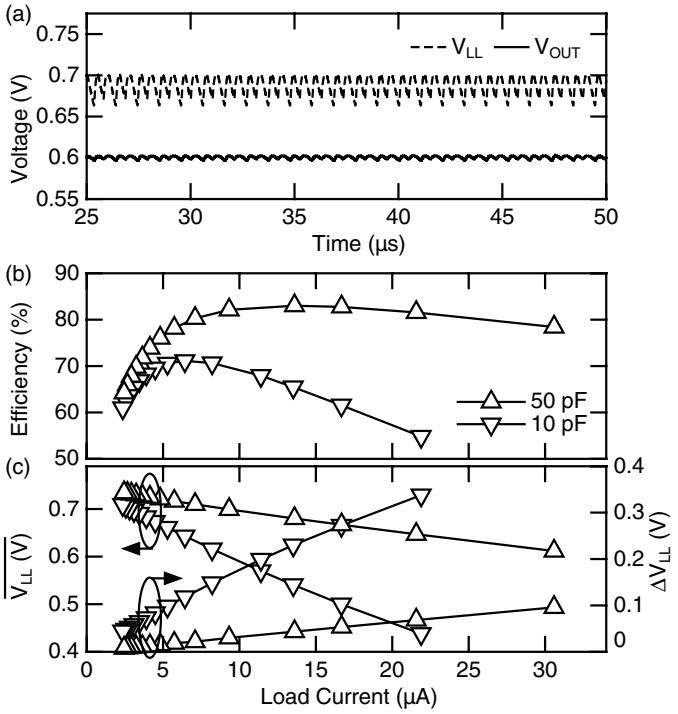

Fig. 8. Operation of total circuit: (a) waveforms of V_{LL} (SC converter output) and V_{OUT} (series regulator output), (b) efficiency of SC converter as a function of output current, and (c) average $\overline{V_{LL}}$ and ripple ΔV_{LL} as a function of output current.

tested the performance of the circuit with a SPICE simulation. All the capacitors were the same size, and the load resistance changed from 20 to 300 kΩ. The on-resistance of the switch was about 3 kΩ.

Figure 6 shows the simulated results of clock waveforms ϕ_1 and ϕ_2. Reference current I_{BIAS} was set to 50 nA. The oscillation frequency was 950 kHz. Two phase switching clocks ϕ_1 and ϕ_2 were obtained without any overlapping. The power consumption of the circuit was extremely low, 0.75 μW, with a 1.5 V power supply. These results indicate that the clock signals are on state separately and that the circuit can be constructed with ultralow-power consumption.

Figure 7 plots the transfer curves of the series regulator, i.e., output voltage V_{OUT} and monitored current I_1 as a function of input voltage V_{LL}. The reference current I_{REF} was set to 10 nA. The circuit operated correctly at a V_{LL} of 0.6 V or higher. The waveforms of V_{LL} (SC converter output) and V_{OUT} (series regulator output) are plotted in Fig.8 (a), with capacitance $C_{1-4} = 50$ pF, $I_{REF} = 10$ nA, and output current (load current) $= 13$ μA. The average and the ripple voltage are 0.68 V and 40 mV_{pp} for V_{LL} and 0.60 V and 5 mV_{pp} for V_{OUT}. Figure 8 (b) plots the efficiency of the SC converter, and Figure 8 (c) shows the average and ripple of V_{LL} as a function of the output current, with C_{1-4} as a parameter. With the C_{1-4} of 50 pF, the SC converter showed a maximum efficiency of 83 %, including the power of the clock generation circuit at a 13 μA output current. The total power efficiency of the circuit from the input supply to the series regulator output is 73 %. This can be improved by using a large value for C_{1-4}. A larger capacitance needs a larger area but can be implemented on the periphery of the chip. And the MOS capacitor can be used to reduce the area for C_2 and C_4. On the basis of these results, we can develop subthreshold-operated LSIs, including microwatt smart-sensor LSIs.

IV. Conclusion

We developed an on-chip high-efficiency switched capacitor DC–DC voltage converter and a series regulator for ultralow-power subthreshold MOS LSIs. The circuit was found to operate correctly by the 0.35-μm standard CMOS process. Simulation results of the circuits showed that the power efficiency of the SC DC–DC converter is 83 % and that the total efficiency is 73 % at a 0.68 V output voltage and a 13 μA load current with $C = 50$ pF. The circuit can be used as a power supply circuit for subthreshold CMOS logic circuits.

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