A Subthreshold Memory Cell utilizing Nonlinear Characteristics of Positive-feedback Operational Transconductance Amplifier

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We propose a memory cell consisting of a subthreshold positive-feedback operational transconductance amplifier (OTA) biased by leak currents of MOS FETs, aiming at the development of ultra-lowpower logic systems for battery-powered nodes of sensor networks, by sacrificing the operational frequency (to around Hz to kHz). The fundamentals were proposed in [1], and in this report we optimize the circuit in terms of power consumption, latency, and error rates. The cell has potential tolerance against the threshold mismatch, as compared with conventional memory cells consisting of a pair of inverter latches. Through extensive SPICE (Monte-Calro) simulations with 0.35-um standard CMOS parameters including practical variations of the devices, we show i) the static noise margin (SNM), which is defined by a hysteresis width and output amplitudes of the OTA, is proportional to the magnitude of the power supply voltage, ii) the maximum delay in rise and fall times was blow 1 us at V_{dd} = 1.8 V with the standard deviation of MOS FETs (22 mV), which implies that the cell is able to operate at 1 MHz clocks, iii) error rates (the number of error bits per trial for data writing) of the proposed circuit 0 % (among 1000 trials) until V_{dd} > 0.4, iv) the power consumption at V_{dd} = 0.5 V for sequential reading and writing operations was around 50 fW@1 kHz, whereas the conventional memory cells consumed 0.2 pW for the same experimental setups, and v) the maximum delay at V_{dd} = 0.5 V was around 200 ms. Furthermore, we show experimental results of the fabricated chips (AMS 0.35-um CMOS process). The fabricated circuit exhibited expected memory operations except for the maximum delay (was around 1 s) and the maximum power consumption (was about 10 times larger than the expected power in simulations). We will evaluate the difference between the simulation and experimental results, and will discuss the effects of die-to-die mismatches on the memory operations.

References

[1] Utagawa A., Asai T., and Amemiya Y., "Stochastic resonance in simple analog circuits with a single operational amplifier having a double-well potential," Nonlinear Theory and Its Applications, vol. 2, no. 4, pp. 409-416, 2011.