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High-Fidelity Pulse-Density Modulation with Noisy Neuromorphic Circuits based on Model of Vestibulo-Ocular Reflex

Akira Utagawa†, Tetsuya Asai, and Yoshihito Amemiya

Graduate School of Information Science and Technology, Hokkaido University.
Kita 14, Nishi9, Kita-ku, Sapporo, 060-0814 Japan.
Phone:+81-11-706-7147, Fax:+81-11-706-7890
† email: utagawa@lalsie.ist.hokudai.ac.jp

Abstract

We designed a neuromorphic electrical circuit that performs pulse-density modulation at high fidelity by using noises in electrical circuits. We constructed a network circuit based on a neural network model proposed by Hospedales *et al* [1]. They regarded that the neural network used for the "vestibulo-ocular reflex" (VOR) could respond to temporal signals whose frequencies were higher than the maximal firing frequency of a single neuron in a network. In other words, the network could increases fidelity to the input of the network. They reported that this characteristic could be achieved by implications of temporal and spatial noises in neurons. We use temporal and spatial noises of electrical circuits to improve fidelity to input based on their model. Multiple neuron circuits are connected in parallel, and temporal noises and spatial noises are artificially implemented to mimic environmental noises and devices mismatches in electrical circuits. Through circuit simulations, we demonstrate that our proposed circuit with noises can conduct a temporal signal whose frequency is higher than the frequency that a single neuron circuit can conduct.

1. Introduction

Our purpose is to explore possible ways to construct an electrical circuit that can perform high-speed information processing with slow devices. Regarding this point, neural networks seem to be a possible choice because they are considered to perform high-speed parallel information processing with neuron elements which are relatively slower than CMOS transistors. In recent study, Hospedales *et al*. reported that a neural network with temporal noises and spatial noises in neurons that was used to perform "vestibulo-ocular reflex" (VOR) could conduct a temporal signal whose frequency was higher than operation frequency of a single neuron in networks [1]. VOR stabilizes the visual field by moving the eyeballs in such a way that compensates for rotations of the head. They reported that this function could be achieved by using temporal and spatial noises of neurons. Figure 1 shows a simple schematic of the model. The four neurons ($N = 4$) represented by the open circles are connected in parallel. All the neurons accept common input and generate spike output i (i: neuron number). The output of the network is given by summing of outputs of all the neurons. When no noises are applied to this network, all the neurons generate spike output at the same time (phase). However, when they are affected by temporal noises ξ_i and spatial noises δ_i, they no longer can generate spike output at the same time. It represents that the network shows asynchronous firing and it can thus respond to relatively faster input signal than a single neuron.

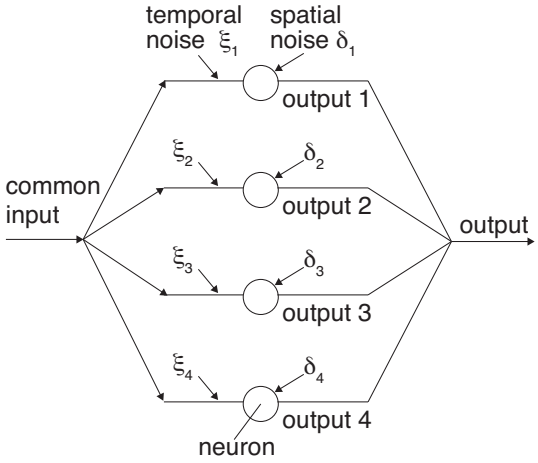

Figure 1: Neural network model of VOR

The operation frequency in electrical circuits of a single device is limited by several conditions that derive from physical limitations. Electrical circuits are often limited by power consumption or chip area size especially in mobile appliances or sensor appliances. Information processing done by the brain is considered to have an energy-efficient structure. The architecture observed in the brain may provide possible solutions to electrical engineering. Further more, electrical-circuit en-

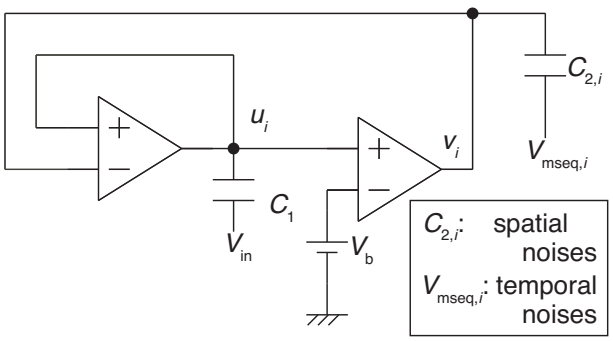

Figure 2: Wilson-Cowan neuron circuit

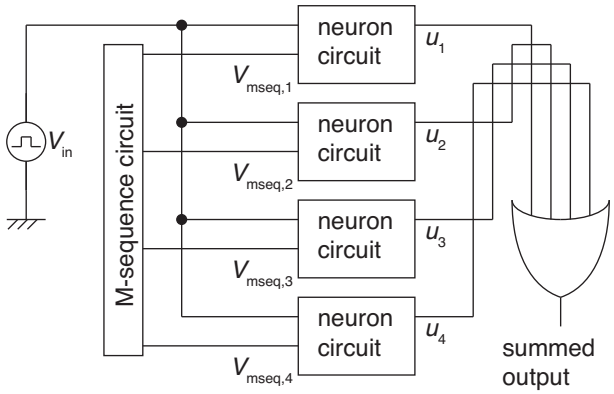

Figure 3: Neural network circuit

gineers often try to reduce or eliminate the effects of noises and device mismatches of transistors because these effects degrade circuit characteristics and they even cause erroneous circuit operation. Typical circuit designs to reduce these effects often require additional transistors and larger transistors (= larger chips and greater power consumption), which makes it more difficult to meet the specification. Here, by implementing Hospedales et al.'s model in electrical circuits, noises and device mismatches in these circuits could be utilized to improve operations while group of slow devices could achieves faster operation. We constructed a simple neural-network circuit to confirm the improvements in fidelity and we then demonstrate that the operation frequency of a noisy network circuit is higher than that of a noiseless network circuit.

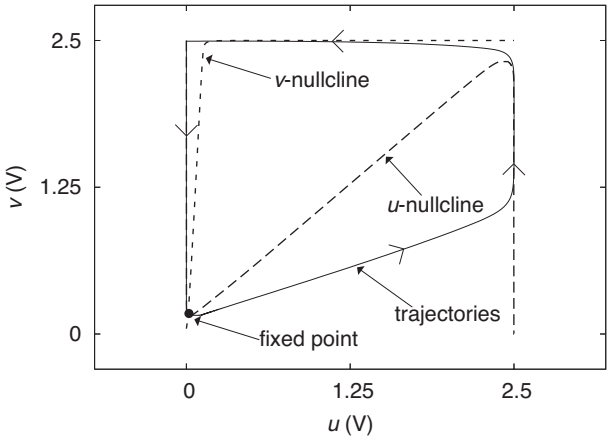

Figure 4: Trajectories and nullclines for u and v of single neuron circuit

2. CMOS pulse-density modulator implementing neural network model of VOR

Based on the results obtained by Hospedales *et al*. [1], we developed a network circuit consisting of multiple MOS neuron circuits. Figure 2 shows a schematic of an i-th neuron circuit based on the Wilson-Cowan oscillator model [2]. The u_i and v_i represent system variables of the i-th oscillator, V_{b} the bias voltage, C_1 and $C_{2,i}$ the capacitance, and the $V_{\mathrm{mseq},i}$ the pseudo noise voltage generated by a 4-bit M-sequence circuit. The $V_{\mathrm{mseq},i}$ fluctuates the trajectories occurred in the circuit so that phase advance or delay of the oscillator occurs. The oscillator circuit accepts pulsed input voltage V_{in} and generates a spike event (v_i) when V_{in} increases. After a spike is generated, the circuit can hardly generates s spike even if an input signal is applied for a certain period. This period is called the "refractory period" in biology. After this period, it can generate spike events. This means that when the input frequency is higher than a certain threshold, the circuit can not correctly responds to the input. The length of the refractory period is mainly determined by a capacitance $C_{2,i}$. Figure 3 has a schematic of a network circuit. Four neuron circuits were used for our preliminary research (N = 4). The spatial noises in the model can be mimicked by setting $C_{2,\mathrm{i}}$ to different values. Consequently, each neuron circuit has a slightly different refractory period and has a slightly different limitations in intrinsic frequency. These neurons accept identical (correlated) pulsed signal V_{in} and uncorrelated pulsed signal $V_{\mathrm{mseq,i}}$. Because the noises signal $V_{\mathrm{mseq},i}$ drastically change phases by applying fluctuations to v_i, no firing events by neurons occur with the same timing although common input is applied to all the neurons. This means that the probability of the network firing remains high when noises are applied. The entire output is expressed by the logical summing of all neurons' output events with the OR logic circuit.

3. Simulation results

Figure 4 shows the nullclines and trajectories for a noiseless ($V_{\mathrm{mseq,i}}$ = 0 V) single (N = 1) neuron circuit. In simula-

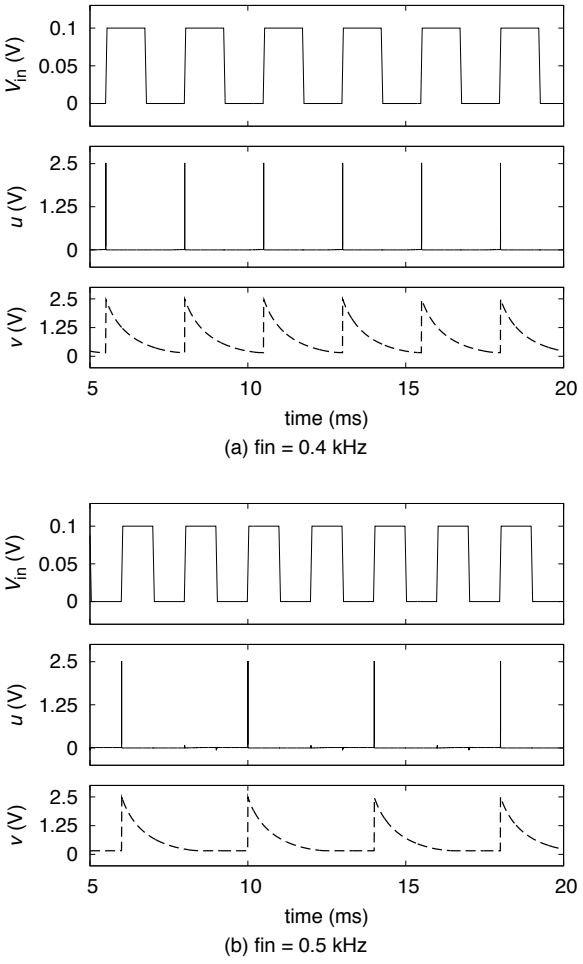

Figure 5: Simulated response of single neuron

tions of the simgle neuron circuit, C_1 was 100 fF, $C_{2,1}$ was 300 fF, V_{dd} was 2.5 V, and the clock frequency of the M-sequence circuit was set to 0.5 kHz.V_b was set to 0.12 V so that the neuron circuit would stay stable if input signal V_{in} did not contain a temporal signal. We confirmed the excitatory operation after pulse input was applied as shown in Fig. 4. Figure 5 shows simulated responses of a noiseless oscillator (V_{mseq} = 0) to variable input-pulse frequencies (f_{in}). When f_{in} was 0.4 kHz [Fig. 5 (a)], the neuron could conduct input pulses and generates spike output in response to the rise time of input pulses. However, when f_{in} was 0.5 kHz [Fig. 5 (b)], the neuron could not conduct these input pulses and the neuron generated spike events once every two input pulses. We confirmed that the single neuron circuit could responds to temporal signals whose frequencies is lower than 0.4–0.5 kHz. To visualize the relationship between pulse input frequency f_{in} and the spike output frequency f_{out}, we plotted the dependence of f_{out} on f_{in} in Fig. 6. The open squares represent the simulation results and the solid line is an approximated curve

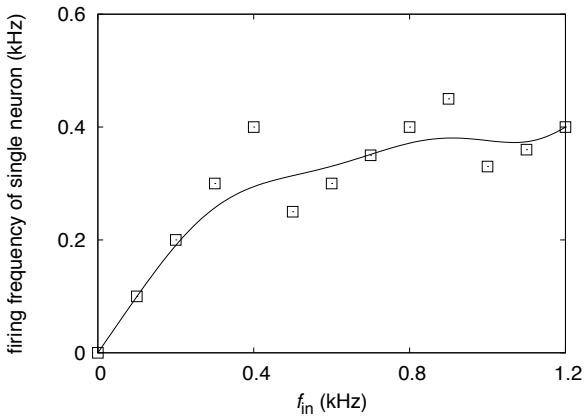

Figure 6: Dependency of firing frequency of single neuron on input frequency

for these data. As seen from the figure, the circuit could conduct input whose frequencies were 0–0.4 kHz while it could not conduct input whose frequencies were over 0.4 kHz. This limitation depended on capacitance $C_{2,i}$.

We will now discuss what the effect noises had in our network circuit. We conducted simulation with and without noises. No noises meant that none of the four neuron circuits accepted temporal noises given by $V_{mseq,i}$ and each capacitance $C_{2,i}$ had the same value (300 fF). Applying noises meant that all the neuron circuits accepted individual temporal noises ($V_{mseq,i}$) and the value of $C_{2,1}, C_{2,2}, C_{2,3}$, and $C_{2,4}$ were set to correspond to 280, 290, 300, and 310 fF. Raster plots and output of the network circuit in Fig. 7 indicate the performance of the circuit without noises [Fig. 7 (b)] and with noises [Fig. 7 (c)]. We set f_{in} to 1.2 kHz which is faster than operation frequency of a single neuron circuit (0.4 kHz). Figure 7 (a) shows the input signal. The symbols $+, \times, *$, and $\square$ in Fig. 7 correspond to firing events for neurons 1, 2, 3, and 4, and the vertical line represents the firing events of the whole network circuit. When no noises were applied, the four circuits had exactly the same characteristics; thus all their outputs is identical as shown in Fig. 7. This meant that the output of the four neurons had the same value as the output of a single neuron. This also meant that even if more neurons were employed the performance of the network circuit would not be improved. When noises were applied to neurons, their individual response to common input was different due to noises because they dynamically changed the state of each neuron. The outputs of a single neuron are not periodic and seem to be random. However, output could express an input signal. The output of a network circuit with noises has an irregular signal that is caused by noises. We showed that a noisy circuit surpasses a noiseless circuit in its response to an input signal. Dependence of f_{out} on f_{in} plotted in Fig. 8

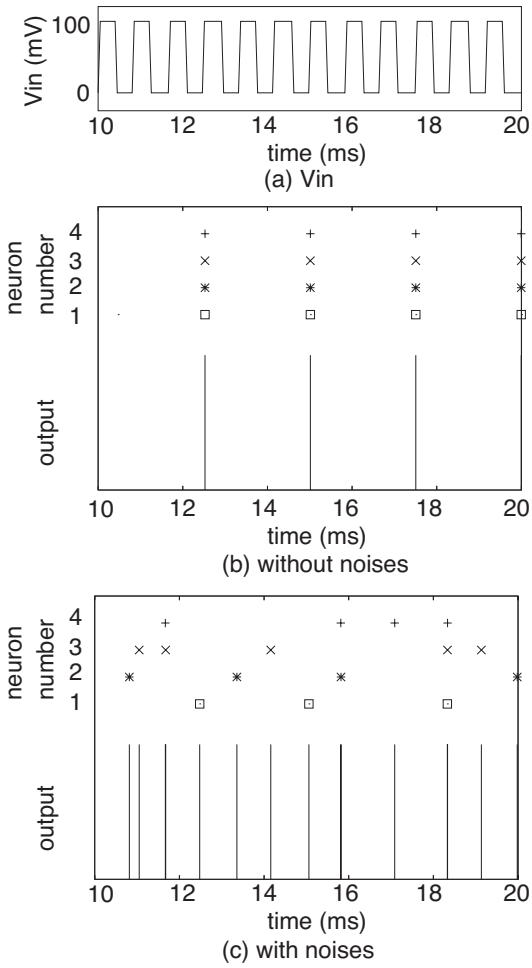

Figure 7: Raster plots and output event of network circuit

demonstrate the performance. The open squares plot results for the circuit without noises and the filled circles show results for the circuit with noises in Fig. 8. The solid black line represents where $f_{\text{in}} = f_{\text{out}}$. The noiseless circuit had the same characteristics as shown in Fig. 6. This circuit could respond to 0.4 kHz, which is the upper limit frequency of a single neuron circuit, and it could not respond to frequencies that were higher than the limit frequency of a single neuron. When noises were applied to the circuit, the same characteristics were qualitatively confirmed with the model. When f_{in} was low f_{out} was higher and almost same value (0.5 kHz). When f_{out} was high f_{out} was linear to f_{in}. It was difficult to achieve these characteristics without noises. Applying random initial conditions may achieve the same characteristics in the noiseless circuit because random initial conditions give phase delay and firing events occur randomly for each neuron. However, even if random initial conditions were applied their phases were synchronized by a common input signal whose

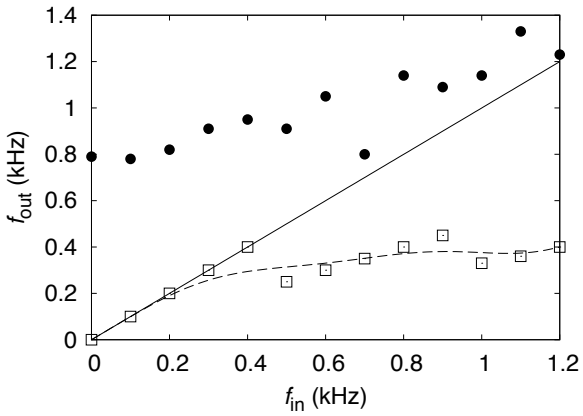

Figure 8: Dependence of f_{out} on f_{in}

frequency and amplitude do not have a fixed value.

4. Conclusion

We developed a neuromorphic circuit with high fidelity in its output spike train based on the Vestibulo-Ocular Reflex (VOR) model. We constructed a network circuit consisting of neuron circuits, an M-sequence circuit, and an OR logic circuit. We confirmed that a single neuron circuit could operate up to 0.4 kHz and it operated incorrectly over 0.4 kHz. When four neurons were used in simulations, the network without noises had the same characteristics while the network with noises had higher performance than that without noises. The noisy network could operate correctly at 1.2 kHz and we confirmed that fidelity could be increased by noises. We were forced to limit the operation frequency of the neuron circuit that we introduced in this report forced to a certain value due to the size of capacitance in the circuit. We plan to use a subthreshold CMOS circuit that allows an ultra-low power circuit even though device mismatches strongly degrades circuit characteristics.

References

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