A Memristor-based Synaptic Device having an Asymmetric STDP Time Window

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We propose an elemental device for possible brain-inspired hardware; *i.e.*, analog synaptic devices (circuits) that consists of a bipolar ReRAM (memristor), MOS FETs and a capacitor only. The device has an ability to update the synaptic conductance according to the spike timing of pre and post neuron devices.

One of the key issues for implementing neural networks on semiconductor integrated circuits is "how we implement non-volatile analog synapses". Many engineers have tried to design analog synaptic devices based on existing flash-memory technologies, but they had difficulties in designing associate controllers for electron injection and ejection as well as increasing the limited frequency of the rewriting. Using possible memristive nano-junctions, a digital-controlled neural network has been introduced by Snider in 2007 [1]. We here propose yet-another analog approach; *i.e.*, a memristor (ReRAM)-based analog synaptic circuit, for possible neuromorphic computers.

Our key idea is to assign a capacitor in one terminal of a memristor, as shown in Fig. 1. An input node of the memristor accepts voltage spikes ($V_{\rm pre}$ in Fig. 1), and the PSP node ($V_{\rm PSP}$) is connected to a gate terminal of a MOSFET (M_0) and a capacitor ($C_{\rm pre}$). This capacitor is charged or discharged by the input spike via the memristor. Because a MOSFET has nonlinear characteristics between the gate voltage and the drain current, by integrating the drain currents of M_0 on the other (membrane) capacitor, we obtain different membrane potentials for different conductance of the memristor. If the membrane potential exceeds a given threshold voltage, a post neuron circuit (standard integrate-and-fire circuit) generates a voltage spike ($V_{\rm post}$ in Fig. 1). At the same time, the PSP node is shunted by an additional MOSFET (M_1). Therefore, due to the potential difference across the memristor, the conductance is increased, which exhibits spike-timing-dependent plasticity (STDP) in our memristor synapse (for the timing difference $\Delta t > 0$) , *i.e.*, the timing difference between pre-synaptic and post-synaptic spikes results in the differential synaptic weights (differential conductance of the memristor). To obtain $\Delta t < 0$ responses, we employed additional MOS FETs (M_2 to M_5). M_4 and M_5 acts as a source-common amplifier and exhibits large time delay, which can be controlled by $V_{\rm b}$, on voltage V_1 upon the falling edge of $V_{\rm post}$ because $C_{\rm gd}$ is amplified by the Mirror effect. When M_7 is turned on (just after the firing of $V_{\rm post}$), $I_{\rm MAX}$ is mirrored to M_3 via current mirrors M_8-M_9 and M_3-M_6. At the same time, if M_2 is turned on by $V_{\rm pre}$, $V_{\rm PSP}$ is increased. Consequently, at the falling edge of $V_{\rm pre}$, conductance of the memristor is decreased. Figure 2 shows simulation results of our synaptic device. In the simulations, we assumed characteristics of a fabricated memristor (bipolar ReRAM) of NiO thin films (Pt-NiO-Pt) and a discrete MOS device (2SK1398 and 2SJ184) and a capacitor (0.1 μF). The result clearly showed that the differential conductance ($\Delta G_{\rm MEM}$) was modified by the difference of spike timings of pre- and post-synaptic neurons (Δt).

Reference

[1] G.S. Snider, Nanotechnology, 18(36), 365202, 2007.

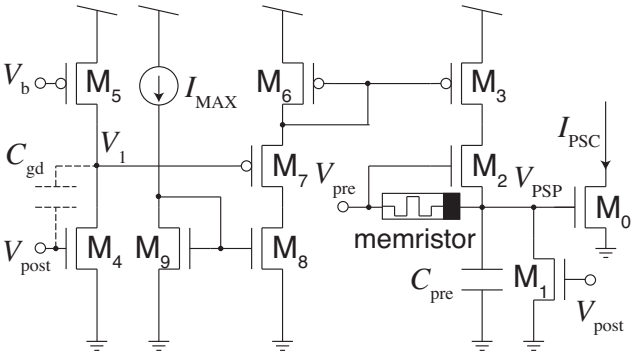

Fig. 1. Proposed memristor STDP circuit.

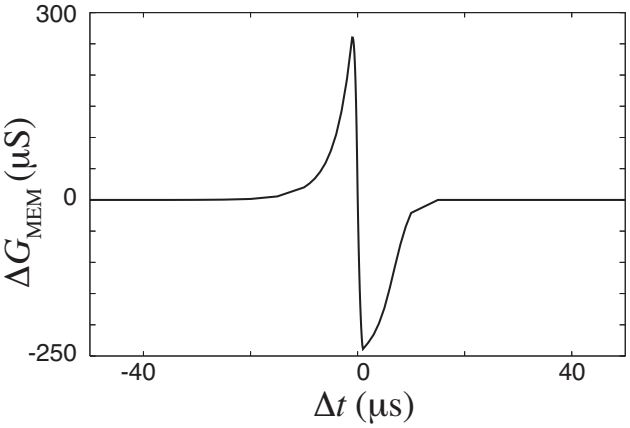

Fig. 2. Simulated asymmetric STDP results.

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