Ultralow-Power Temperature-Insensitive Current Reference Circuit

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Summary

One of the promising areas of research in microelectronics is the development of ultralow-power smart sensor LSIs that operate in the subthreshold region. To step toward these ultralow-power subthreshold CMOS-LSIs, we first need to develop a constant current reference circuit that can operate with ultralow-power dissipation. Using this reference circuit, we can construct pre- and post- signal processing circuits with ultralow-power dissipation for the smart sensors. In this work, an ultralow-power constant current reference circuit with low temperature dependence is proposed. This circuit consists of a constant-current subcircuit and a bias-voltage subcircuit, and it compensates for the temperature characteristics of mobility (μ), thermal voltage ($V_T = k_B T/q$), and threshold voltage (V_{TH}) in such a way that the reference current has small temperature dependence. As an example in the design of setting the output reference current at 100 nA, a SPICE simulation demonstrated that total power dissipation is 1.1 μW and the variation in the reference current can be kept very small within ±4% in a wide temperature range from -20 to 100 °C.

Circuit configuration

The current reference circuit we propose consists of a constant-current subcircuit and a bias-voltage subcircuit. The latter supplies a bias voltage to the former. Figure 1 shows the constant-current subcircuit. It is based on the basic β–multiplier self biasing circuit and uses a MOS resistor instead of a passive resistor. We operate all MOSFETs in the subthreshold region except for the MOS resistor in the strong-inversion and triode region. The current flowing in this circuit is determined by the ratio of M_A and M_B and the resistance of the MOS resistor. Temperature coefficient (TC) of the current can be expressed by the temperature dependence of the mobility, thermal voltage, and threshold voltage. Figure 2, where a TC reported by other group[1] is also plotted, shows that it can be made small value and set to zero at room temperature by adjusting V_B to an appropriate value. Buck et.al. proposed a CMOS reference circuit without resistors[2]. Their circuit is modified in order to operate in the subthreshold region and generate a fixed bias-voltage for the current subcircuit. Figure 3 shows the entire configuration of the circuit. To ensure the same current flowing in M_A and M_B, the source-coupled amplifier is used to hold the same drain voltages V_A and V_B of the transistors M_{P1} and M_{P2}. To use the source-coupled amplifier, we adapt a cascade configuration of nMOSFETs in the constant-current subcircuit.

Results

Figure 4 shows the simulated results for the current as a function of temperature. In this simulation the ratio of K_B/K_A was set to 1.06. The reference current and total power dissipation is 97.7 nA and 1.1 μW, respectively, at the room temperature. The variation in the reference current and the bias-voltage can be suppressed within ±4 % and ±1 %, respectively, in the temperature range from -20 to 100 °C. Figure 5 shows the simulated reference current and bias-voltage as a function of the supply voltage. The circuit can operate at a low power supply voltage of 1.2 V. The variation in the current and the bias voltage can be suppressed within ±4 % and ±1 %, respectively, in the supply voltage range from 1.2 to 3 V. Table 1 summarizes the performance of this current reference.

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[1] Henri J. Oguey, and Daniel Aebischer, "CMOS Current Reference Without Resistance", *IEEE J. Solid-State Circuits*, Vol.32, No.7, pp. 1132-1135, Jul. 1997.

[2] Arne E. Buck, Charles L. McDonald, Stephen H. Lewis, and T.R. Viswanathan, "A CMOS Bandgap Reference Without Resistors", *IEEE J. Solid-State Circuits*, vol. 37, No.1, pp.81-83, Jan., 2002.

Figures

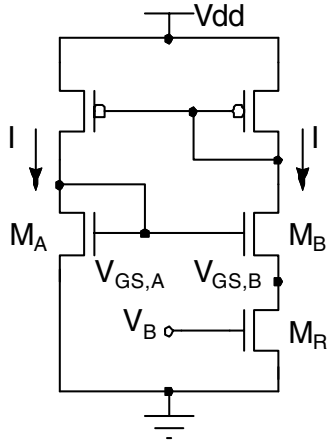

Fig. 1: Proposed constant-current subcircuit.

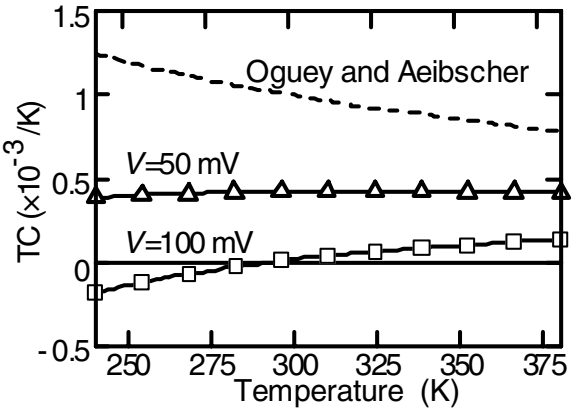

Fig. 2: Calculated Temperature Coefficient of the current we proposed.

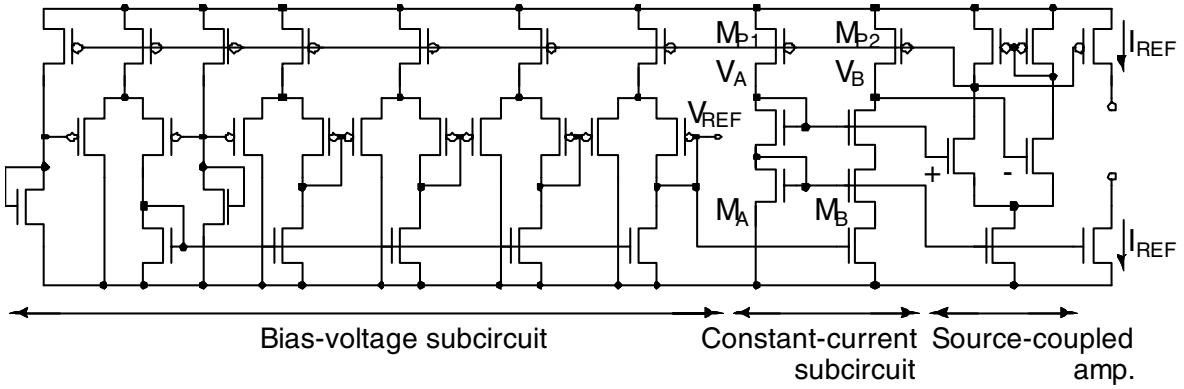

Fig. 3: Current reference circuit consisting of bias voltage subcircuit and constant current subcircuit.

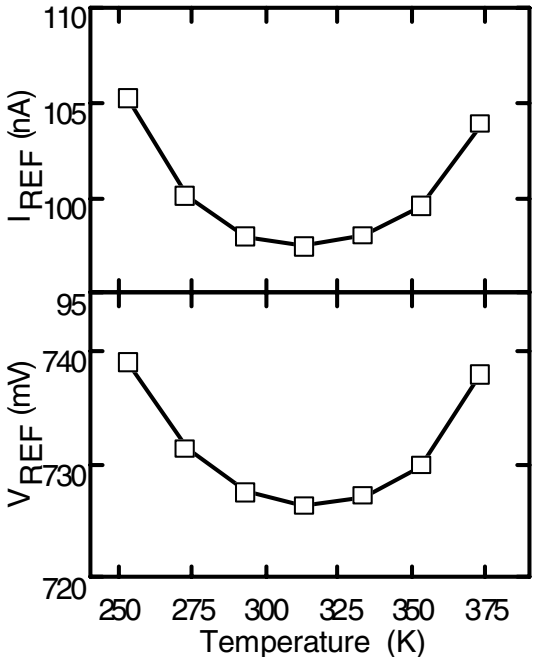

Fig. 4: Simulated output reference current and bias voltage as a function of temperature.

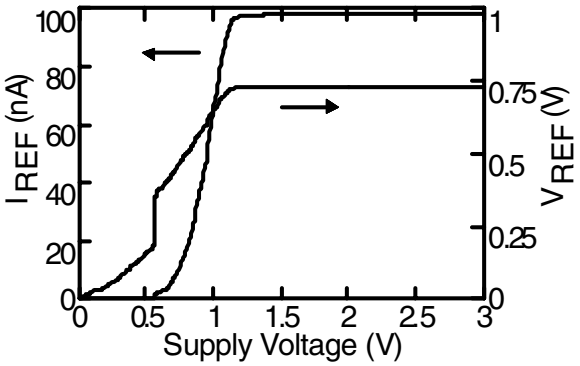

Fig. 5: Simulated output current and bias-voltage as a function of supply voltage.

Tab. 1: Performance summary.

Technology	0.25um, 1P5M CMOS
V_{DD}	1.5 V
I_{REF}	97.7 nA (T = 25 °C)
V_{REF}	727 mV (T = 25 °C)
Power	1.1 μW (T = 25 °C)
$\Delta I_{REF}/I_{REF}$	±4 % (T = –20~100 °C)
	±0.60 % (V_{DD} = 1.2~3 V)
$\Delta V_{REF}/V_{REF}$	±1 % (T = –20~100 °C)
	±0.19 % (V_{DD} = 1.2~3 V)