# A hardware depressing synapse and its application to contrast-invariant pattern recognition

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**Abstract:** Analog circuits for depressing synapses are proposed for emulating the dynamic properties of neural networks using dynamic neurons. Although the circuits have few MOS transistors, they mimic well the dynamic properties of depressing synapses. A simple neural network using depressing synapses is introduced for evaluating the performance of hardware depressing synapses. We show that a device using the neural network can perform contrast-invariant pattern recognition based on a neuromorphic processing architecture.

**Keywords:** dynamic synapse, depressing synapse, neuromorphic VLSI

## 1. Introduction

Silicon circuits that mimic the nervous systems of insects and other animals represent the future of neurocomputing [1, 2]. They can perform various neural functions because the microstructures of a nervous system are replicated on their silicon chips. A number of neural VLSIs have already been developed including silicon neurons that emulate cortical pyramidal neurons [2], FitzHugh-Nagumo neurons with negative resistive circuits [3], and artificial neuron circuits based on by-products of conventional digital circuits [4, 5, 6]. Since recent functional models of spiking neural networks tend to use integrate-and-fire neurons (IFNs), neuromorphic engineers have developed hardware neural systems with several types of IFN circuits to investigate the effect of spike timing and synchrony on the network's computational properties.

In addition to the hardware IFNs, dynamic synapses have also attracted the attention of neuromorphic engineers who focus mainly on the dynamic implications of the neurons. A recent model of the layer IV circuitry, which accounts for several contrast-dependent nonlinearities in cortical responses, suggests that synaptic depression contributes to solveing the problem of contrast-invariant orientation tuning [7]. Based on this suggestion, Bugmann showed that the strength of a time-averaged current injected into the soma by using a spike train is independent of its frequency, which implies that the response strength of a target neuron depends only on the number of active inputs [8]. This property is very useful for artificial vision systems, particularly for preprocessing natural images. We propose an analog circuit that uses Bugmann's model. Our aim is the development of potential applications of neuromorphic VLSIs to artificial vision. We show by circuit simulation that such a circuit can perform contrast-invariant pattern recognition.

## 2. Analog CMOS circuits for dynamic synapses

A synapse whose conductivity changes based on the firing rate or spike timing of presynaptic neurons is called a dynamic synapse [9, 10]. The change in weight of dynamic synapses is caused by short-term changes in the transmitter discharge and regeneration cycle at the terminal of presynapses rather than by learning on a network level. These synapses produce excitatory postsynaptic potential (EPSP) and inhibitory postsynaptic potential (IPSP) by integrating the output of the presynaptic neurons. A signal is conducted to a postsynaptic neuron through EPSP and IPSP. When the firing frequency of the presynaptic neurons increases so that the sequential changes in EPSP and IPSP can no longer follow the input, the efficiency of signal conduction to the postsynaptic neurons drops. Thus, this synapse functions as a low-pass filter. Because presynaptic neuron output is depressed and conducted to the postsynaptic neurons, such a synapse is called a "depressing synapse" and a synapse acting inversely is called a "facilitating synapse".

Figure 1 shows a prototype diagram of a depressing synapse circuit. Depending on the type of connection with the postsynaptic neurons, depressing synapses are classified as excitatory or inhibitory. The excitatory (inhibitory) synapse circuit charges (discharges) the membrane ($C_{\mathrm{m}}$) of the postsynaptic neuron and the membrane potential rises (falls). Each synapse circuit receives input current $I_{\mathrm{in}}^{(\mathrm{e,i})}$ and generates EPSP and IPSP. EPSP and IPSP are converted into electric current by MOS transistors $\mathrm{M_e}$ and $\mathrm{M_i}$. The current charges and discharges the membrane ($C_{\mathrm{m}}$) of the postsynaptic neurons. When the MOS transistors operate in their subthreshold region, the excitatory postsynaptic current (EPSC: electrical current of $\mathrm{M_e}$) and inhibitory postsynaptic current (IPSC: electrical current of $\mathrm{M_i}$) are

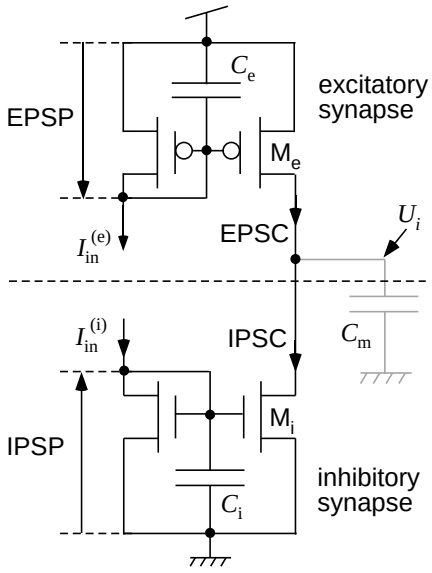



Figure 1: Excitatory and inhibitory depressing synapse circuits.

given by

$$\text{EPSC} = I_0 \exp(\kappa \text{EPSP}/V_\text{T}), \quad (1)$$
$$\text{IPSC} = I_0 \exp(\kappa \text{IPSP}/V_\text{T}), \quad (2)$$

where $I_0$ and $\kappa$ are process-dependent parameters, $V_T = kT/q$ ($k$ is Boltzmann's constant, $T$ is absolute temperature, $q$ is electron charge). The dynamics of the excitatory and inhibitory synapses are

$$C_\text{e}\frac{d\text{EPSP}}{dt} = -I_0 \exp(\kappa \text{EPSP}/V_\text{T}) + I_\text{in}^{(\text{e})}, \quad (3)$$
$$C_\text{i}\frac{d\text{IPSP}}{dt} = -I_0 \exp(\kappa \text{IPSP}/V_\text{T}) + I_\text{in}^{(\text{i})}, \quad (4)$$

where $C_\text{e}$ ($C_\text{i}$) expresses the capacitance between the excitatory (inhibitory) synapse and soma.

The depressing synapse circuit (Fig. 1) is simple, but it is problematic for handling impulse inputs (pulse width of spiking does not depend on firing frequency). This synapse circuit integrates input pulses by charging and discharging two capacitances ($C_\text{e}$ and $C_\text{i}$). When the capacitance becomes high (integration over a long period), the maximum amplitude of the output pulse drops and the pulse widens. Therefore, the maximum amplitude of the output pulse is depressed, but the efficiency per spike (i.e., the amount of electrical charge per spike) does not change between the presynapses and postsynapses. We thus propose a depressing synapse circuit in which the efficiency per synapse is depressed based on the increase in firing rate whose construction is easy. The firing rate can be increased as high as the input of the constant pulse width.

Figure 2 shows a depressing synapse constructed by combining a current mirror and common-source amplifier. When there is no input ($I_\text{in} = 0$), voltage $V_\text{e}$ of junction A is zero. Therefore, transistor $\text{M}_1$ is in an on

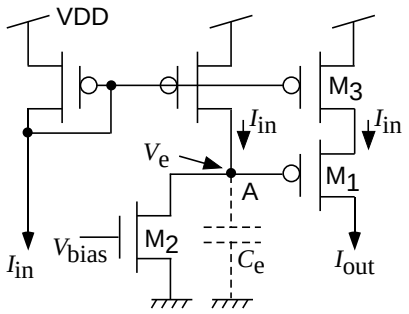



Figure 2: Depressing synapse circuits for impulse input.

state. When there is input ($I_\text{in} > 0$), $V_\text{e}$ increases and $\text{M}_1$ enters an off state. Therefore, the current mirrored to output $I_\text{out}$ through transistor $\text{M}_1$ and $\text{M}_3$ is zero. Because there is parasitic capacitance $C_\text{e}$ at junction A, the increase in $V_\text{e}$ has a short-time delay. Therefore, $\text{M}_1$ enters an on state for a short time, and the circuit outputs pulsive current $I_\text{out}$. When the input current becomes zero again, $\text{M}_1$ discharges the electrical charge of parasitic capacitance $C_\text{e}$, and $V_\text{e}$ returns to zero. If the pulsive current is given at a short interval, subsequent spikes enter before $V_\text{e}$ returns to zero. Because $\text{M}_1$ is not completely on, the amplitude of the output spikes becomes small based on the magnitude of $V_\text{e}$ (when $V_\text{e}$ increases, the amplitude of the output spikes decreases). Therefore, the efficiency per spike (amount of electrical charge per spike) decreases. Because the current of transistor $\text{M}_2$ increases monotonically based on the increase in gate voltage $V_\text{bias}$, when $V_\text{bias}$ increases, the time until $V_\text{e}$ returns to zero decreases. By adjusting voltage $V_\text{bias}$, it is thus possible to change the time constant of the depression.

We propose yet another dynamic synapse circuit that exhibits both depressing and facilitating properties. First, a current integrator, as shown in Fig. 3 (a), is constructed. Input $I_\text{in}$ from the presynaptic neuron is transferred to junctions A and B by the current mirror ($\text{M}_{\text{p}1}$ to $\text{M}_{\text{p}3}$), and capacitors $C_\text{e}$ and $C_\text{i}$ are charged; transistors $\text{M}_\text{e}$ and $\text{M}_\text{i}$ discharge the electrical charge of capacitors $C_\text{e}$ and $C_\text{i}$. When the firing cycle of the presynaptic neuron becomes shorter than the charging and discharging time constant of the current integrators, the mean value of $V_\text{e}$ (or $V_\text{i}$) eventually increases. In this circuit, drain voltages $V_\text{e}$ and $V_\text{i}$ of transistors $\text{M}_\text{e}$ and $\text{M}_\text{i}$ take values below $4V_\text{T}$ (MOS transistor does not operate in saturation condition). Therefore, the dynamics at junctions A and B in Fig. 3 are as follows:

$$C_\text{i}\dot{V}_\text{i} = I_\text{in} - I_0 e^{\kappa V_\text{g}^{(\text{i})}/V_\text{T}} \left(1 - e^{-V_\text{i}/V_\text{T}} + V_\text{i}/V_0\right)$$
$$C_\text{e}\dot{V}_\text{e} = I_\text{in} - I_0 e^{\kappa V_\text{g}^{(\text{e})}/V_\text{T}} \left(1 - e^{-V_\text{e}/V_\text{T}} + V_\text{e}/V_0\right).$$

Outputs ($V_\text{e}$, $V_\text{i}$, and $V_\text{spike}$) of Fig. 3(a) are given to a translinear multiplier-divider [11]. The input-output characteristic of the multiplier-divider is

$$I_\text{out} = \frac{I_\text{e}}{I_\text{i}} I_\text{in},$$

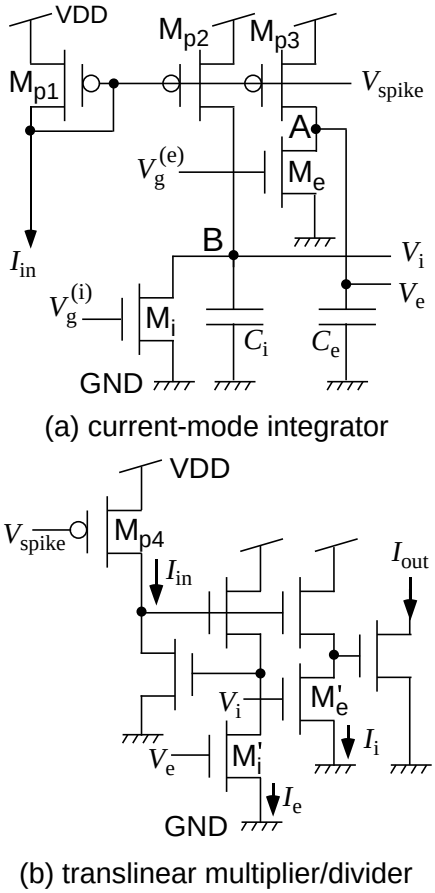



Figure 3: Depressing and facilitating synapse circuits.

and if transistors $M'_e$ and $M'_i$ operate in saturation conditions, the output current of the circuit is

$$I_{out} = \frac{e^{\kappa V_e/V_T}}{e^{\kappa V_i/V_T}} I_{in}.$$

Input $I_{in}$ from the presynaptic neuron received from the circuit of Fig. 3(a) is given to the multiplier-divider through the current mirror sharing $V_{spike}$; $V_e$ and $V_i$ of Fig. 3(a) are given to the gates of transistors $M'_e$ and $M'_i$ in Fig. 3(b). When $V_e > V_i$, the multiplier-divider amplifies input from the presynaptic neurons, and when $V_e < V_i$, output is restricted. If the amplitude of the input spiking current from the presynaptic neurons is constant and $C_i = C_e$, the integration quantity of the current at junctions A and B is determined only by the current of transistors $M_e$ and $M_i$. The current of these transistors increases monotonically based on the increase in gate voltages $V_g^{(e)}$ and $V_g^{(i)}$ of $M_e$ and $M_i$, so when the gate voltage increases, the time constant of the integration circuit decreases. Therefore, if $V_g^{(e)} > V_g^{(i)}$, the time average of $V_i$ becomes larger than that of $V_e$ every time spiking input is given, and the gain of the translinear multiplier-divider decreases. If $I_{in}$ and $I_{out}$ are the output of the presynaptic neurons and the input of the postsynaptic neurons, this circuit functions as a depressing synapse. If $V_g^{(e)} < V_g^{(i)}$, the mean value of $V_e$ eventually becomes larger than that of $V_i$, and the gain of the translinear multiplier-divider increases. This circuit thus functions as a facilitating synapse. Switching between the functions of depression and facilitation is based on the balance between the magnitudes of $V_g^{(e)}$ and $V_g^{(i)}$.

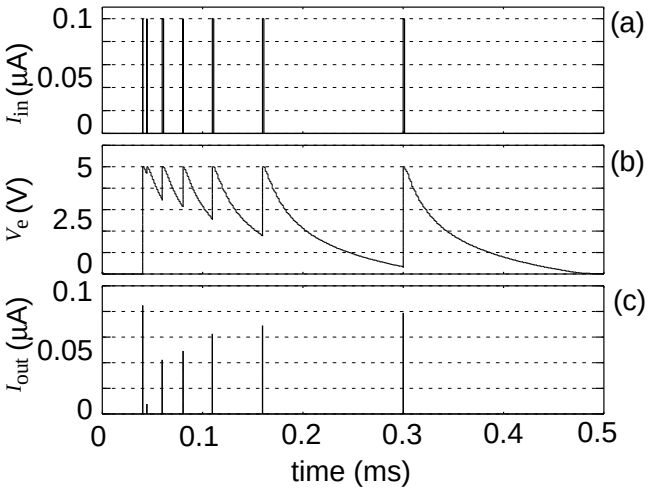



Figure 4: Simulated operation of depressing synapse circuits.

# 3. Evaluation

We simulated the operation of the dynamic synapse circuits using the HSPICE circuit simulator with the transistor parameters of AMIS 1.5-$\mu$m CMOS technology provided by MOSIS. Minimum-size transistors (channel width 2.3 $\mu$m; channel length 1.5 $\mu$m) were used.

Figure 4 shows example operation of the depressing synapse circuit ($V_{bias}$ = 0.3 V, input pulse width = 10 $\mu$s, pulse amplitude = 0.1 $\mu$A). Input current $I_{in}$ was given to the circuit as spikes by changing the spike interval [Fig. 4(a)]. The first spike was given at $t$ = 40 $\mu$s. Subsequent spikes were given at $t$ = 44, 60, 80, 110, 160, and 300 $\mu$s. When the inputs were given successively in a short time (around 4 to 50 $\mu$s in Fig. 4(a), the amplitude of the output pulse was depressed [Fig. 4(c)]. As the interval widened, $V_e$ approached zero [Fig. 4(b)], and the amplitude of the output pulse returned to the initial value. Figure 5 shows the change in amplitude of the output spike against the input spike interval. As the spike interval became shorter, the amplitude of the output pulse decreased.

Figure 6 shows example operation of depressing and facilitating synapse circuits ($C_e = C_i$ = 10 pF, input pulse cycle = 1 ms, pulse width = 10 $\mu$s, pulse amplitude = 1 nA). As designed, when $V_g^{(e)} > V_g^{(i)}$ and spike input $I_{in}$ [Fig. 6(a)] was given, the difference between $V_e$ and $V_i$ increased due to the increase in the number of spikes ($V_i < V_e$), and $I_{out}$ decreased based on the input of the spiking row [Fig. 6(b)], with $V_g^{(e)}$ = 0.3 V and $V_g^{(i)}$ =

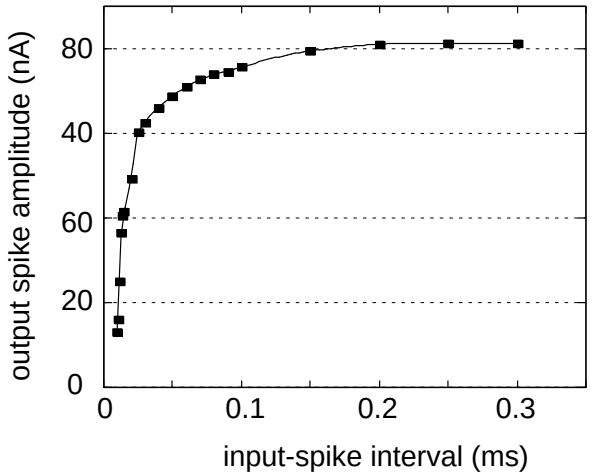



Figure 5: Change in output spike amplitude against input spike interval.

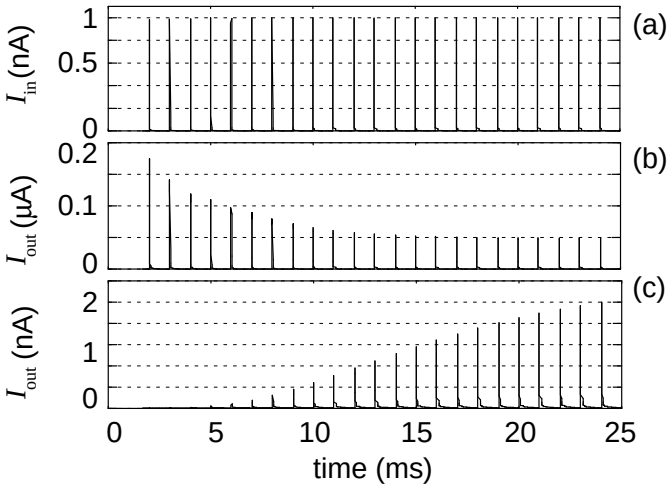



Figure 6: Operations of depressing and facilitating synapse circuits.

0.2 V. In contrast, for $V_g^{(e)} < V_g^{(i)}$, $I_{out}$ increased based on the input of the spiking row [Fig. 6(c)], with $V_g^{(e)} =$ 0.1 V and $V_g^{(i)} = 0.3$ V. When the input was cut off, the current gain gradually returned to the initial value.

# 4. Active pattern-recognition network using depressing synapses

We assume the simple network illustrated in Fig. 7. Many spiking neurons are connected to a postsynaptic neuron. Active neuron outputs spike at a constant rate, and inactive neuron outputs do nothing. The postsynaptic neuron outputs a spike for $V_{SOMA} > V_{TH}$ and resets $V_{SOMA}$ after firing. $V_{SOMA}$ increases in proportion to the number of presynaptic active neurons. Therefore, this network can discriminate the number of presynaptic active neurons if threshold $V_{TH}$ is set corresponding

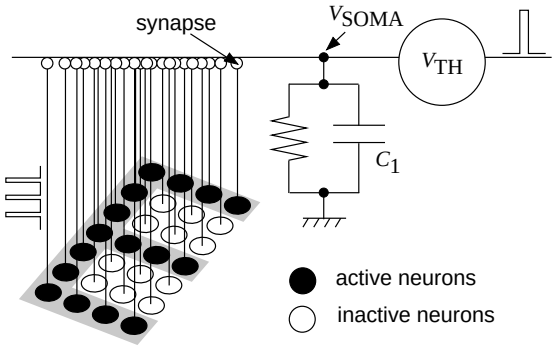


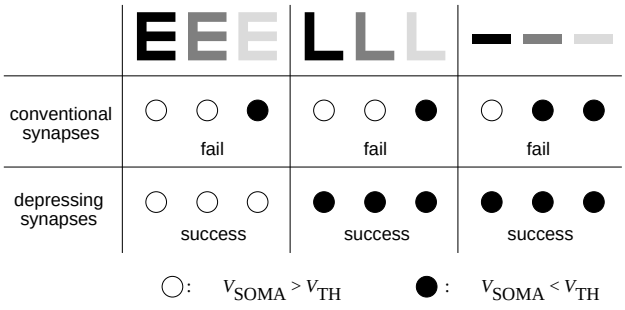

Figure 7: Active pattern discrimination circuits using depressing synapses and spike neurons.

to the number of active neurons.

$V_{SOMA}$ also increases in proportion to the firing frequency of the spiking neurons. For example, we assume that the pulse amplitude and pulse width of the input spikes and the leak from $V_{SOMA}$ are constant independent of the firing frequency of the input spikes. The value of $V_{SOMA}$ produced by 50 active neurons with a firing frequency of 20 Hz is the same as the value of the potential produced by 10 active neurons with a frequency of 100 Hz. Therefore, the ability of the network shown in Fig. 7 to discriminate the number of presynaptic active neurons deteriorates greatly due to the change in firing frequency. Using the depressing synapse thus makes the discrimination performance independent of the firing frequency (discrimination performance is improved) [8].

If several spikes enter the depressing synapse successively in a short period (a case of high-firing-frequency neurons), the efficiency per spike (the amount of electrical charge that flows into $C_1$ of Fig. 7) drops. Even if the number of input spikes increases with the firing frequency, the value of $V_{SOMA}$ does not change greatly because the efficiency per spike is lowered. The discrimination performance of the network thus becomes independent of the firing frequency. The discrimination result should differ, as shown in Table 1, between using the depressing synapse and not using it. Here, presynaptic neurons are located in two dimensions, as shown in Fig. 7. The active neurons form patterns such as "E", "L", and "-". The number of neurons is the largest for "E" and the smallest for "-". We assume that the threshold is set midway between "E" and "L". The firing frequency is expressed by grayscale letters in the table. Closer to black, the firing frequency is high; closer to white, the firing frequency is low. In a network not using depressing synapses, even in "E", which intrinsically does not fall below threshold, $V_{SOMA}$ does not exceed the threshold at a low firing frequency. In "L" and "-", which intrinsically does not exceed the threshold, $V_{SOMA}$ should exceed the threshold at a high firing frequency. In a network using depressing synapses, because a depressing synapse lowers the efficiency per spike at a high firing input frequency, an increase in

Table 1: Difference in discrimination performances with and without depressing synapses.



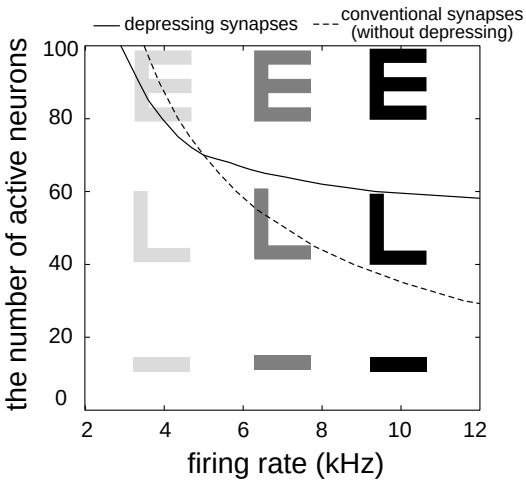




Figure 8: Simulated firing frequencies when $V_{SOMA}$ exceeded the threshold for the first time (number of synapses = 100).

$V_{SOMA}$ is independent of the firing frequency. The network should thus discriminate the number of active neurons independently of the firing frequency. We implemented this network electronically using the dynamic synapse circuit we designed and found that its performance approaches the ideal case (Table 1).

To confirm improvement in discrimination performance in a large-scale network, HSPICE simulation was conducted for a network having 100 depressing synapse, like that in Fig. 2. We assumed that the presynaptic active neurons form patterns such as "E", "L", and "-". "E" takes 90 neurons, "L" takes 50, and "-" takes 10. The input is a pulse with an amplitude of 1 nA and a width of 10 $\mu$s. The time constant of the postsynaptic neuron was 2 ms. We evaluated the performance of the network with both conventional and depressing synapses. The threshold was set at the value of $V_{SOMA}$ produced by 70 active neurons with a firing frequency of 5 kHz assuming a pattern midway between "E" and "L". Threshold $V_{TH}$ was 0.2 V when depressing synapses were used and 1.97 V when conventional synapses were used.

The firing frequencies when $V_{SOMA}$ exceeded the threshold for the first time are plotted in Fig. 8. The discrimination result was the same as shown in Table 1 except for conventional synapses with few active neurons (shown by the "-") at the highest frequency. This indicates that the network with the proposed depressing synapse circuit performed as well as the ideal one irrespective of the use of analog CMOS devices. The letter closest to black expresses the firing of each active neuron at 10 kHz, the letter closest to white at 4 kHz, and the letter of the intermediate shade at 7 kHz. When the depressing synapse was not used, correct discrimination could not be achieved as it was for "E" and "L". Went it was used, correct discrimination was achieved for all patterns. The discrimination performance of the network can thus be improved by using the depressing synapse.

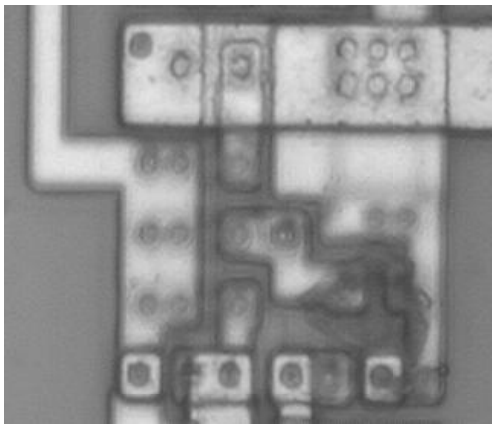


Figure 9: The depressing synapse circuit fabricated by a 1.5-$\mu$m CMOS process.

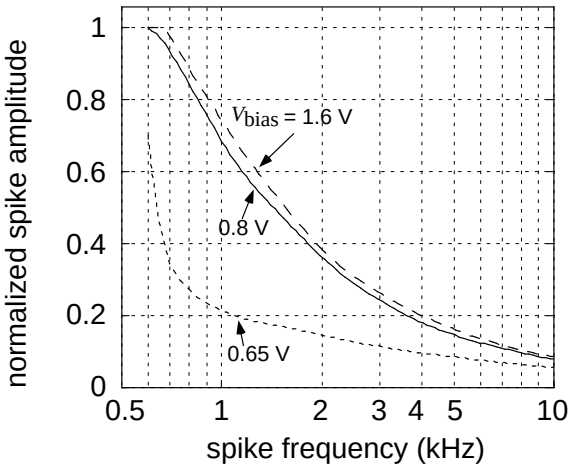



Figure 10: Experimental results for the change in output spike amplitude against input spike frequency.

We fabricated a prototype chip using a 1.5-$\mu$m CMOS process (MOSIS, vendor: AMIS). Figure 9 shows a micrograph of the depressing synapse circuit. The circuit took up a total area of 36 $\mu$m $\times$ 35 $\mu$m.

Figure 10 shows experimental results of the depress-

ing synapse circuit representing the change in amplitude of the output spike against the input spike frequency. As the spike frequency increased, the amplitude of the output pulse decreased, as expected. The degree of depression was changed successfully by controlling bias voltage $V_{\text{bias}}$.

## 5. Conclusion

We described an analog dynamic synapse circuit as the first step toward developing neuromorphic architectures. We also described an electronically implemented functional network using the circuit that has synapses and neurons with dynamic properties. The network is for active pattern recognition based on extracted information about the firing frequency from input information. We evaluated the performance of the networks using both electronic circuit simulation and fabricated chip. We found that the network can achieve active pattern recognition and that the discrimination performance is improved by using depressing synapses.

In an analog electronic circuit, information is expressed by converting a natural physical quantity into a physical quantity (voltage or current), so noise directly affects the information handled, making it very important to take measures against noise. In a natural environment without noise measures, spiking neurons will likely generate erroneous spiking. Tolerance of changes in the firing frequency means that the network cancels out this erroneous spiking. A network for active pattern recognition bust be tolerant of noise. We showed that our network for active pattern recognition is tolerant of noise although no special noise measures are taken. Although the problem of noise cannot be completely overcome, our finding that analog circuits can be made naturally noise-tolerant by constructing network circuit based on an organism structure is very promising in the development of antinoise measures in analog LSIs.

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