Multi-valued logic circuits consisting of single-electron devices

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Abstract

R. A. Kiehl *et al*.[1] proposed a novel method of using phase –locking in single-electron devices to realize Tunneling-Phase digital logic. In this paper, we utilize mutual interaction and phase-locking in single-electron oscillators to design multi-valued digital logic circuits. We propose a basic cell consisting of capacitively coupled single-electron oscillators to realize a 4-valued logic circuit.

Single-electron oscillators

Single-electron devices operate by controlling the transport of individual electrons, through Coulomb blockade phenomenon, illustrated in detail by H. Grabert and M.H. Devoret [2]. The constituent circuit of this research, the single-electron oscillator (Fig. 1(a)) consists of a tunneling junction C_j, connected to a bias voltage V_d through a high resistance R. If the bias voltage is higher than the tunneling threshold voltage $e/2C_j$, the oscillator portrays self-induced oscillations as shown in Fig. 1(b). The node voltage gradually increases as the junction capacitance C_j is charged through resistance R (curve AB), until it achieves the threshold, where an electron tunnels from the ground to the node leading to a discrete jump in its voltage, by $\triangle V=-e/C_j$. Coupled oscillators mutually interact with each other. For instance in a capacitively coupled oscillator circuit, electron tunneling in one oscillator produces a discrete jump in the entire circuit node voltages, creating a time lag between consecutive tunneling events in the coupled oscillators. Fig. 2(a) shows an example of such coupled identical oscillators. The two oscillators are biased to the same voltage V_{dd}. Their operation is shown in Fig. 2(b). If an electron tunnels from the ground to node 1, the voltage of node 1 decreases by $\triangle V_1=e/C_j$, while that of node 2 decreases by $\triangle V_2=\triangle V_1(C/(C+C_j))$. This drop in the voltage of node 2 delays tunneling in oscillator 2, leading to alternate tunneling in the two oscillators.

Realizing multi-valued tunneling phase logic

Fig. 3 (a) shows a basic Tunneling Phase Logic (TPL) unit. The TPL unit consists of a single-electron oscillator connected to an AC pump signal. The pump provides a sinusoidal voltage with amplitude V_p, and frequency two times faster than the single-electron oscillator. With the use of 5 TPL units, we constructed a 4-valued logic circuit (Fig. 3(b)). Oscillators 1-4 are capacitively coupled to oscillator 5. The pump signal sub-harmonically locks tunneling in the oscillators (i.e. in every period of the pump signal, a single tunneling event takes place in each and every oscillator). Due to mutual interaction amongst the oscillators, a time (phase) lag between tunneling events in the four oscillators 1-4 occurs. Adjusting this phase lag, we can obtain a multi-valued logic system.

Simulation results

Fig. 4 shows the simulation results. The dots represent the timing at which tunneling takes place in oscillators 1-4, while the vertical axis shows the phase lag between the pump signal and tunneling events in the corresponding oscillator. With this circuit, we confirmed that the four oscillators tunnel at almost even intervals, between 0-π. To express the logic values in terms of phase, we subdivide the entire phase lag θ in to quadrants: $0 < \theta_0 < \pi/4 < \theta_1 < \pi/2 < \theta_2 < 3\pi/4 < \theta_3 < \pi$. Expressing these 4 phase ranges with logic values 0, 1, 2, and 3 respectively, we could obtain a 4-valued logic circuit. Controlling the logic value of a specific oscillator is done with the use of an external trigger signal. In Fig. 4, we set the logic value of oscillator 1 to 3. The other 3 oscillators were locked to the remaining 3 logic values, as shown in Fig. 4.

References

1. R. A. Kiehl and T. Ohshima. Bistable locking of single-electron tunneling elements for digital circuitry. Appl. Phys. Lett., 67(17):2494–2496, 1995.

2. H. Grabert and M.H. Devoret, *Single Charge Tunneling*, Plenum Press, New York, 1992.

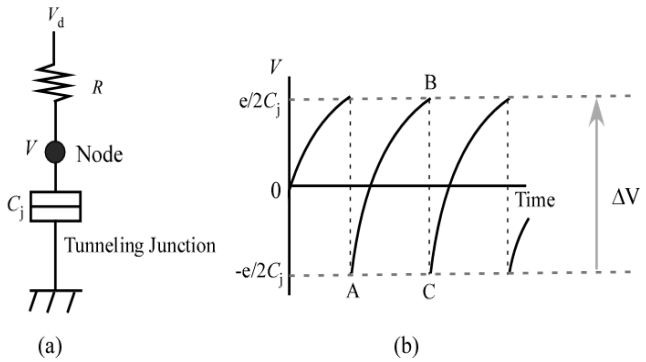

Fig. 1 Single-electron oscillator (a) Structure (b) Self-induced oscillations

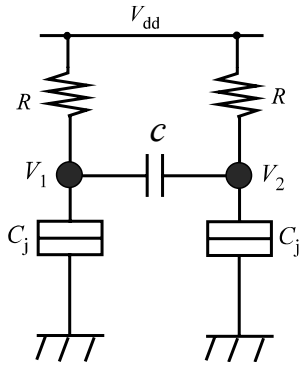

Fig. 2 (a) Coupled oscillator circuit (parameters: V_{dd}=10mV, C_j=10aF, C=2aF, R=1MΩ)

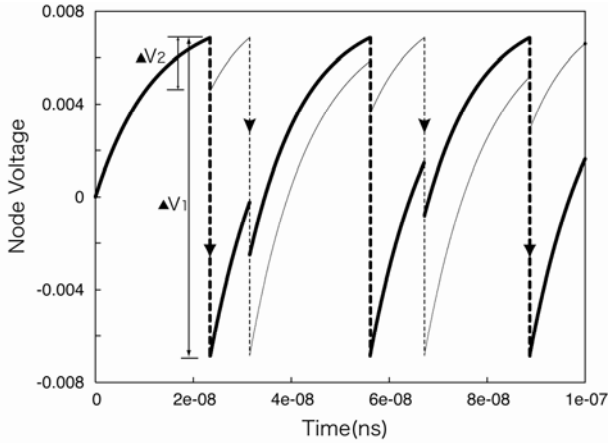

Fig. 2(b) Operation of the coupled oscillator circuit. Solid lines show gradual increment of node voltages: Thick lines for voltage V_1 (node 1) and thin lines for V_2 (node 2). Dotted lines show discrete change in node voltage due to electron tunneling.

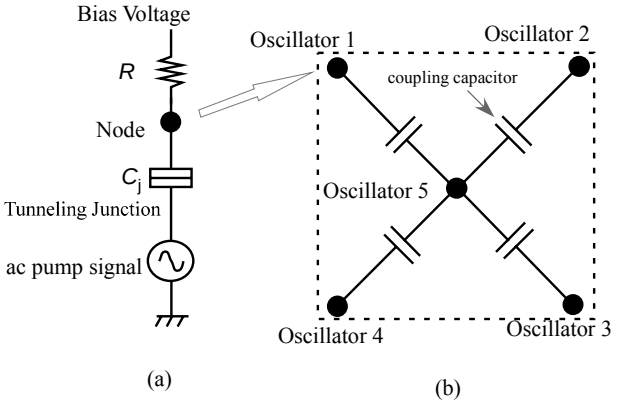

Fig. 3: (a) Single-electron Tunneling Phase Logic (TPL) unit (b) Multi-valued logic circuit consisting of 5 TPL units

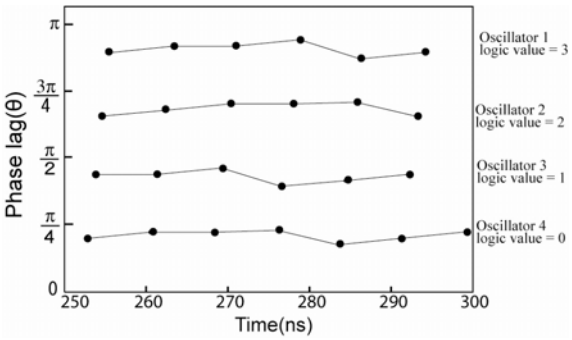

Fig. 4: Simulation results. Tunneling phase lag for oscillators 1-4.