Watchdog Circuit for Product Degradation Monitor using Subthreshold MOS Current

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1. Introduction

We developed a new electronic circuit to monitor degradation in consumer products such as medical goods, farm products, food, beverages, and so on. In general, the expiration date is carefully specified to guarantee quality before shipping. However, it is inappropriate to fix the expiration date in advance without knowing their preservation conditions. Degradation in any consumer product should be monitored with an ultra-low-power circuit directly attached to the consumer product. The idea for an expiration date checker, a watchdog circuit, originates from the rate of material degradation being expressed with a rate equation regardless of the mechanisms, such as the chemical reaction. The circuitry attached to each product can monitor its real quality by emulating the amount of degradation based on the activation energy, even if its preservation condition dynamically changes.

2. Overview

Materials degrade based on a thermal chemical reaction; materials A and B react, and then unwanted material C generates. This reaction is expressed as $A + B \rightarrow C$. According to this reaction, the concentration of the unwanted product $[C]$ can be given by

$$[C] = \int_0^{t_1} k[A][B]dt = [A]_0[B]_0 k_0 \int_0^{t_1} \exp\left(-\frac{\Delta E_a}{k_B T(t)}\right) dt, \quad (1)$$

where $[A]_0$ and $[B]_0$ are the initial concentrations of the materials, A and B. The rate constant, k, is given by the pre-exponential factor, k_0, and the activation energy, ΔE_a, for the reaction. k_B is the Boltzmann constant, and T is the absolute temperature. Among many parameters, only temperature ($T(t)$) is a function of time so that the amount of degradation is greatly affected by its thermal history.

We developed a circuit that emulates the degradation of materials by integrating the subthreshold leakage current of a MOSFET. Figure 1 shows the measurement results of the V_{GS}-I_D characteristics. The subthreshold drain current of the MOSFET can be expressed as

$$I_D = I_X \exp\left(\frac{e(V_{GS} - V_X)}{\eta k_B T}\right), \quad (2)$$

where I_X and V_X are temperature independent but process dependent parameters, and η is the subthreshold slope factor. The ratio of two subthreshold currents, I_1 and I_2, can mimic the activation energy. Integrating this ratio with time, one obtains the following equation.

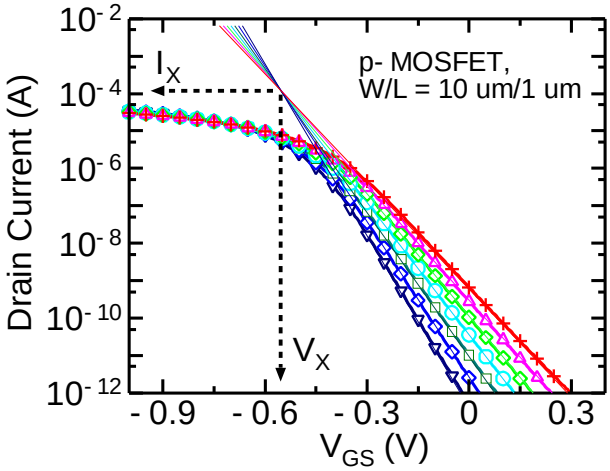

Fig. 1: Measurement results of pMOSFET V_{GS}-I_D characteristics at different temperatures from −20 ℃ to 100 ℃.

$$\int_0^{t_1} \left(\frac{I_1}{I_2}\right) dt = \int_0^{t_1} \exp\left(-\frac{\Delta E}{k_B T(t)}\right) dt, \quad (3)$$

where $\Delta E (= e(V_{GS,2} - V_{GS,1})/\eta)$ is the emulated activation energy, and $V_{GS,1}$ and $V_{GS,2}$ are the gate-source voltages of the subthreshold currents I_1 and I_2, respectively. Equation (3) is proportional to the right-hand side of Equation (1). At given voltages $V_{GS,1}$ and $V_{GS,2}$, the temperature T is the only variable with time. The degradation rate of the material can be monitored from the integrated value.

3. Circuit implementation

To achieve high portability, we adopt the use of a button sized battery with a nominal voltage of 1.5 V. Figure 2 shows the whole circuitry. The whole analog elements work at the subthreshold region to achieve ultra low power consumption.

3.1 Constant current generation circuit

In the ultra-low-power circuit, the reference current should be kept constant even during a wide temperature change. A reference voltage with very little temperature dependence is generated from the four diode-connected pMOSFETs placed in four separate n-wells with their bodies connected to the sources. A p-channel MOS transistor with a large source resistance biased at the reference voltage yields the reference current. A large resistor degenerates the source-gate voltage of the transistor. As the current increases with the temperature, the source-gate voltage decreases, resulting in current suppression, and vice versa. The large resistor consists of 18 pMOSFETs operating in a deep triode region in series connection. The simulated bias current change is suppressed within 1 % variation in the

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temperature range of −25 ℃ to 75 ℃.

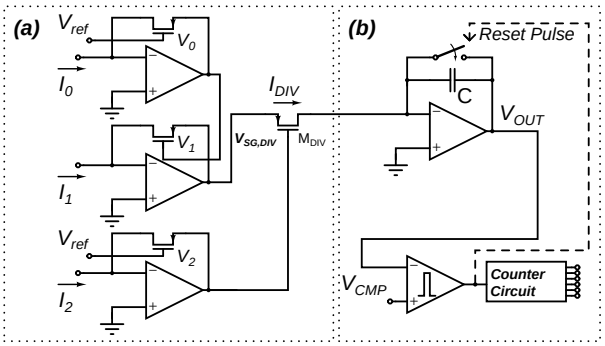

Fig. 2: Block diagram of circuit implementation.

3.2 Elements of the circuitry

Figure 2-(a) shows a subthreshold current divider with logarithm voltage converters consisting of operational amplifiers, feedback transistors, and an anti-log converter transistor[1]. The source-gate voltages of respective feedback transistors, V_0, V_1, and V_2 are the function of the current given as

$$V_i = V_{X_p} + \frac{\eta_p k_B T}{e} \ln\left(\frac{I_i}{I_{X_p}}\right), \quad (i = 0, 1, 2). \tag{4}$$

Taking account of the source-gate voltage of an anti-log converter, $V_{SG,DIV} = V_0 + V_1 - V_2$, the output current I_{DIV} is given by

$$I_{DIV}=I_0 \exp\left(\frac{e(V_{SG,DIV}-V_X)}{\eta_p k_B T}\right)=I_0 \exp\left(-\frac{\Delta E}{k_B T}\right), \tag{5}$$

which emulates the degradation rate with the activation energy of the products. As shown in Figure 2-(b), the capacitor C together with the operational amplifier integrates the current I_{DIV} to generate V_{OUT} given by

$$V_{OUT} = -\frac{1}{C}\int_0^{t_1} I_0 \exp\left(-\frac{\Delta E}{k_B T}\right) dt. \tag{6}$$

A long time current integration requires using a large capacitor, resulting in a large chip. This can, however, be avoided by introducing an iterative integration technique with a small size capacitor. Once the output voltage V_{OUT} surpasses the comparator's reference voltage V_{CMP}, the comparator generates a reset pulse to discharge the capacitor so that the total number of reset pulses is effectively equal to a long integration of the current.

A system using the stated operations provides information on the degree of degradation in products.

4. Measurement results

Figure 3 is a photomicrograph of the chip whose layout area is 510 × 425 μm. Figure 4 shows the simulated output voltage of the integrator at different temperatures from 27 ℃ to 69 ℃. At a given temperature, the output voltage, which is the integration of the emulated current, linearly decreases with operation period, and the slope of the output voltage increases with the operation temperature, both of which are the natural consequences of its operation principle.

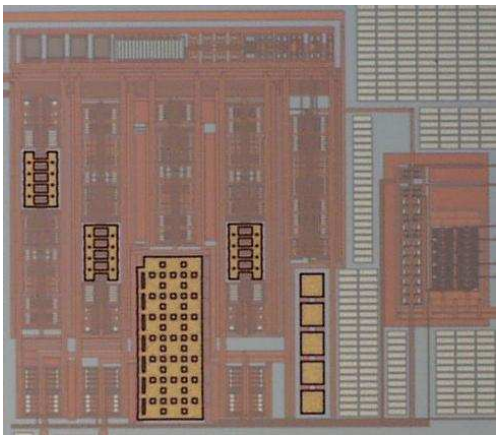

Fig. 3: Chip microphotograph.

These results are quite consistent with the SPICE simulation. In the measurement, the emulated activation energy is set at 50 mV. Note that the circuit operates quite well and that the slope increases as the temperature increases, just as expected.

The simulated power consumption of the circuit is only 3.3 μW at 69 ℃. The button sized battery with 35 mAh ensures that the circuit works for about 1.8 *years*.

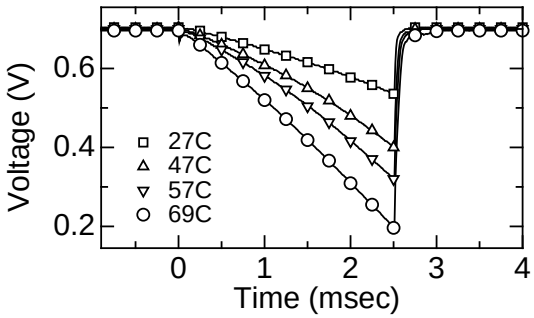

Fig. 4: Measurement results of output voltage for integrator at ΔE = 50 mV.

5. Conclusion

We described a watchdog circuit for a product quality guarantee that dynamically monitors the subthreshold current of a MOSFET. Its operation principle was determined with both a SPICE simulation and measurement of the prototype chip designed with a 0.25-μm CMOS process. The new circuitry was implemented in a tag chip to monitor the degree of degradation for each product upon sale.

References

[1] A.J.Peyton and V.Walsh, "Analog Electronics with OP Amps", CAMBRIDGE UNIVERSITY PRESS, 1993.