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CMOS Voltage Reference Based on the Threshold Voltage of a MOSFET

P-5-4

Ken Ueno, Tetsuya Hirose, Tetsuya Asai, and Yoshihito Amemiya

Department of Electrical Engineering, Hokkaido University,
Kita 14, Nishi 9, Kita-ku, Sapporo, Hokkaido, 060-0814, Japan
Phone: +81-11-706-7147, Fax: +81-11-706-7890, E-mail: k_ueno@sapiens-ei.eng.hokudai.ac.jp

I. Introduction

One of the promising areas of research in microelectronics is the development of ultra-low power analog LSIs that operate in the subthreshold region of MOSFETs [1]. To step toward such LSIs, we first need to develop a low-power voltage reference circuit that can operate with a very small current, several hundreds of nanoamperes or lower. However, with conventional circuitry, such reference circuits need a high resistance of several hundred megaohms, and therefore, they are difficult to implement in a small area on a chip. To solve this problem, we propose a novel voltage reference circuit without resistors. Our circuit combines the positive temperature coefficient of the thermal voltage with the negative temperature coefficient of a MOSFET threshold voltage to achieve a voltage reference with a zero temperature coefficient. The following sections describe this circuit in detail.

II. Circuit Configuration

A. Operation Principle

The voltage reference circuit we propose consists of a current source subcircuit and a bias-voltage subcircuit. The latter supplies a bias voltage to the former. Figure 1 shows the voltage reference circuits we proposed. The current source subcircuit is based on the basic β-multiplier self biasing circuit and uses a MOS resistor $\mathrm{M_{R1}}$ instead of an ordinary passive resistor. The bias-voltage subcircuit accepts the current through pMOS current mirrors and generates the reference voltage. The bias-voltage subcircuit is based on the translinear principle and uses a MOS resistor $\mathrm{M_{R2}}$. We operate all MOSFETs in the subthreshold region except for MOS resistors ($\mathrm{M_{R1}}$ and $\mathrm{M_{R2}}$) in the strong-inversion and deep triode region. The details on the circuit operation are as follows.

The subthreshold MOS current I_D can be expressed as

$$I_D = KI_0 \exp\left(\frac{V_{GS}-V_{TH}}{\eta V_T}\right), \tag{1}$$

where K is the aspect ratio (=W/L) of transistors, $I_0(=\beta(\eta-1)V_T^2)$ is the process-dependent parameter, $V_T(=k_BT/q)$ is the thermal voltage, k_B is the Boltzmann constant, T is the absolute temperature, q is the elementary charge, V_{TH} is the threshold voltage of a MOSFET, and η is the subthreshold slope factor [2].

In the circuit in Fig.1, the current flowing in the circuit I_P is determined by the ratio of $\mathrm{M_1}$ and $\mathrm{M_2}$ and the resistance of MOS resistor $\mathrm{M_{R1}}$, and is given by

$$I_P = \beta(V_{REF}-V_{TH})\eta V_T \ln\left(\frac{K_2}{K_1}\right), \tag{2}$$

where β is the current gain factor. In the bias-voltage subcircuit, gate-source voltages of transistors (V_{GS3} through V_{GS7}) and drain-source voltage of MOS resistor (V_{R2}) form a closed loop with the reference voltage V_{REF}, so we find that

$$\begin{aligned} V_{REF} &= V_{R2}+V_{GS4}-V_{GS3}+V_{GS6}-V_{GS5}+V_{GS7} \\ &= V_{GS4}+\eta V_T \ln\left(\frac{2K_2^3K_3K_5}{K_1^3K_6K_7}\right). \end{aligned} \tag{3}$$

The reference voltage can be expressed by the sum of gate-source voltage $V_{GS4}(=V_{TH}+\eta V_T \ln(I_P/K_4I_0))$ and thermal voltage V_T scaled by the transistor sizes. Because the gate-source voltage and the scaled thermal voltage have negative and positive temperature dependence, respectively, we can obtain a constant voltage with little temperature dependence, adjusting the size of transistors. Note that the threshold voltages and the current gain factors of source-coupled transistor pairs ($\mathrm{M_3}$-$\mathrm{M_6}$, $\mathrm{M_5}$-$\mathrm{M_7}$) and MOS resistor pair ($\mathrm{M_{R1}}$-$\mathrm{M_{R2}}$) can be canceled each other by this circuit configuration.

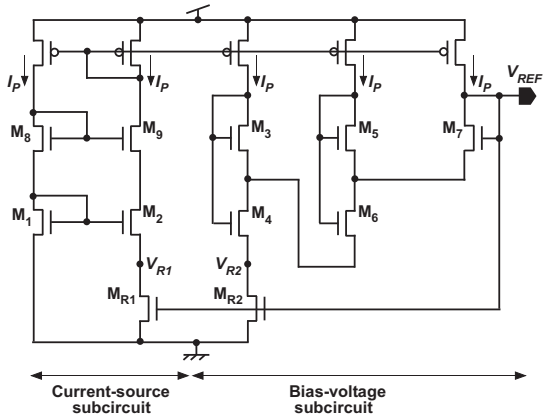

Fig. 1. Schematic of the proposed threshold voltage reference circuit.

B. Temperature Dependence

The temperature dependence of the threshold voltage can be given by

$$V_{TH} = V_{TH0} - \kappa T, \tag{4}$$

where V_{TH0} is the threshold voltage at absolute zero, and κ is the temperature coefficient of the threshold voltage. On the condition where the voltage difference between reference voltage V_{REF} and threshold voltage at absolute zero V_{TH0} is smaller than κT, that is

$$V_{REF} - V_{TH0} \ll \kappa T, \tag{5}$$

temperature coefficient of reference voltage V_{REF} in Eq.(3) is given by

$$\frac{dV_{REF}}{dT} = -\kappa + \frac{\eta k_B}{q}\ln\left\{\frac{6q\eta\kappa}{k_B(\eta-1)}\frac{K_\beta K_2^3K_3K_5}{K_1^3K_4K_6K_7}\ln\left(\frac{K_2}{K_1}\right)\right\}. \tag{6}$$

We can obtain a constant voltage with a zero temperature coefficient by setting the aspect ratios such that $dV_{REF}/dT =$

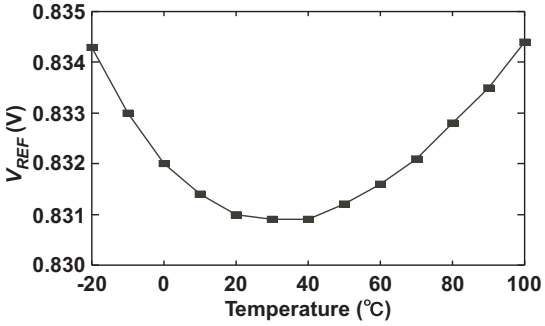

Fig. 2. Simulated output voltage as a function of temperature.

0 in Eq.(6). From Eqs.(2) – (6), the output voltage V_{REF} is given by

$$V_{REF} = V_{TH0} + \eta V_T \ln\left(1 + \frac{V_{REF} - V_{TH0}}{\kappa T}\right) = V_{TH0}. \quad (7)$$

Therefore, the circuit generates the threshold voltage of MOSFET at absolute zero temperature.

III. RESULTS

We confirmed the operation of the circuit by a SPICE simulation with a set of 0.35-μm 2P4M standard CMOS parameters and a 1.5-V power supply. Figure 2 shows output voltage V_{REF} as a function of temperature from –20 ℃ to 100 ℃. An almost constant output voltage can be obtained and average voltage was about 830 mV. The error in the output voltage was within $\pm$0.3 % in the temperature range.

Figure 3 shows average output voltage $\overline{V_{REF}}$ from 1 k-point Monte Carlo simulations assuming process spread and device mismatch in all MOSFETs. Because output voltage V_{REF} monitors the threshold voltage of nMOSFET, average output voltage $\overline{V_{REF}}$ changed with process variation as shown in Fig.3-(a). Figure 3-(b) shows average output voltage $\overline{V_{REF}}$ as a function of the threshold voltage V_{TH}. The output voltage had a linear dependence with threshold voltage. On the contrary, the errors of the output voltage with temperature were quite small and were within $\pm$ 0.3 % as shown in Fig.4. This is because the temperature coefficient of the threshold voltage has little dependence on process variations. The temperature coefficient of the threshold voltage is expressed as

$$\frac{dV_{TH}}{dT} = -(2\eta - 1)\frac{k_B}{q}\left\{\ln\left(\frac{\sqrt{N_c N_v}}{N_a}\right) + \frac{3}{2}\right\} + \frac{\eta - 1}{q}\frac{dE_g}{dT}, \quad (8)$$

where N_a is the channel doping concentration, N_c and N_v are the effective densities of states in the conduction and valence bands, respectively, and E_g is the bandgap energy of silicon [2]. While the threshold voltage of a MOSFET changes significantly with the number of N_a, the temperature coefficient of the threshold voltage changes little because N_a is contained in a logarithmic function.

Table I summarizes the performance of proposed circuits. The simulations showed the maximum power consumption, 1.2 μW at 100 ℃. The change of the output voltage with the supply voltage V_{DD} was within $\pm$ 0.5 % in the range of 1.2 V to 3V.

The reference circuit we proposed refers to the threshold voltage of a MOSFET. Therefore, the absolute value of the output voltage changes significantly with process variation. In other words, the circuit can monitor a process condition of the chip. As an example of the application, the reference voltage can be used as a part of the performance compensation system by monitoring its output voltage, which changes with process condition, not only in subthreshold LSIs, but also in standard CMOS LSIs.

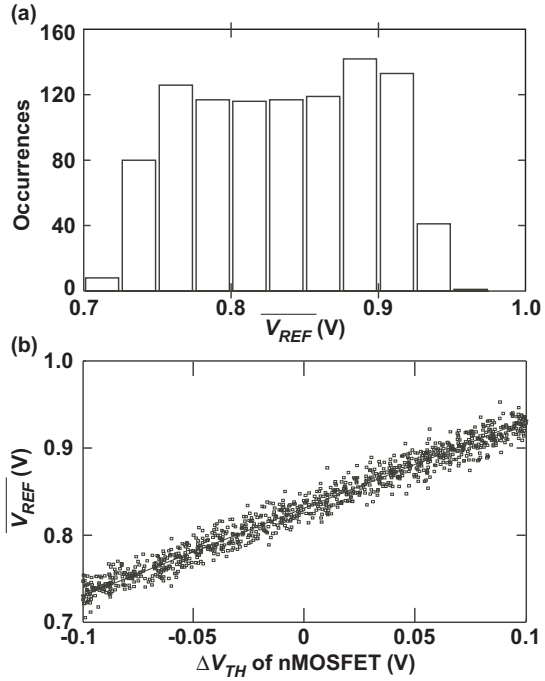

Fig. 3. Simulated results of the output voltage from 1 k-point Monte Carlo simulations. (a) Histogram and (b) threshold voltage dependence of the average output voltage.

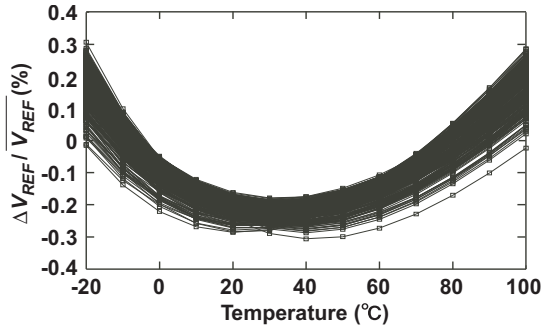

Fig. 4. The errors of the output voltage with temperature derived from Monte Carlo simulations.

TABLE I
PERFORMANCE SUMMARY

Process	0.35-μm, 2-poly, 4-metal CMOS
Temperature range	–20 - 100 ℃
V_{DD}	1.5 V
V_{REF}	830 mV (TYP.)
Power	1.2 μW (T = 100 ℃)
$\Delta V_{REF}/\overline{V_{REF}}$	$\pm$ 0.3 % (T = –20 - 100 ℃)
	$\pm$ 0.5 % (V_{DD} = 1.2 - 3 V)

REFERENCES

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[2] Y. Taur, T.H. Ning, "Fundamentals of Modern VLSI Devices," Cambridge University Press, 2002.