Noise-driven Neural Computing on VLSIs

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Abstract— **This paper provides an overview of the recent development of our noise-driven VLSI circuits whose architectures were inspired by biological nervous systems. Noises are inevitable under natural environment, however, one usually tries to 'attenuate' noises and fluctuations on VLSIs by using, for example, special shielding equipments, precise fabrication process, special layout or circuit techniques, and so on. On the other hand, biological systems certainly 'exploit' noises to increase performances on neural computation. In this paper, some examples of noise-driven neural computing on analog VLSIs are presented, which may show what the noise-driven VLSI circuits can do now, and what they may do in the future.**

I. Introduction

Noise and fluctuations are usually considered as "obstacles" in the operation of both analog and digital circuits, and most strategies to deal with them are focused on the suppression. This paper gives an overview of neural systems that employ different strategies, i.e., neural strategies that can "exploit" the properties of noise to improve the efficiency of operations. First, an inhibitory neural circuit exhibiting noise shaping with subthreshold MOS neuron circuits is introduced. Although device mismatches and external (temporal) noise are given, the circuits exploit the noise properties to perform noise-shaping 1-bit AD conversion (pulse-density modulation). Second, noise-induced synchronization among sub-RF CMOS analog oscillators for skew-free clock distribution is introduced. Independent oscillators are implemented on a chip as distributed clock sources, while the oscillators are synchronized by a common temporal noise. Third, a high-fidelity pulse-density modulator with noisy neuromorphic circuits based on a model of vestibulo-ocular reflex is introduced. When several non-identical pulse-density modulators are collected as noisy neurons, performances on input-output fidelity of the population is significantly increased as compared with that of a single neuron circuit. All the three components above can be implemented by using standard CMOS processes. These strategies may be important in the designs of emerging computer architectures consisting of nanometer-scale (so noise-sensitive) devices.

II. An inhibitory neural network circuit exhibiting noise shaping with subthreshold MOS circuits

Here we aim to develop a possible ultralow-power one-bit analog-to-digital converter (ADC). A one-bit ADC converts analog input signals to digital pulse streams where the analog information is represented in the time domain. This operation is referred to as pulse-density modulation (PDM). A similar operation can be found in spiking neurons , e.g., integrate-and-fire neurons (IFNs) [1]. The firing rate of the neuron increases as the input magnitude incresases. Hence, the spike trains, e.g., the density of spikes per second, represent analog values consisting of 1-0 digital streams. Therefore a one-bit ADC could theoretically be developed by implementing such a neuron circuit on analog VLSIs. In practice, however, it is not easy to develop an ADC with a neuron circuit due to the existence of quantization, static and dynamic noises from the natural environment. The quantization noises can be eliminated by employing a sigma-delta modulator [2], but, eliminating the static noises requires an additional calibration process after chip fabrication, and eliminating dynamic noises requires a special isolation device.

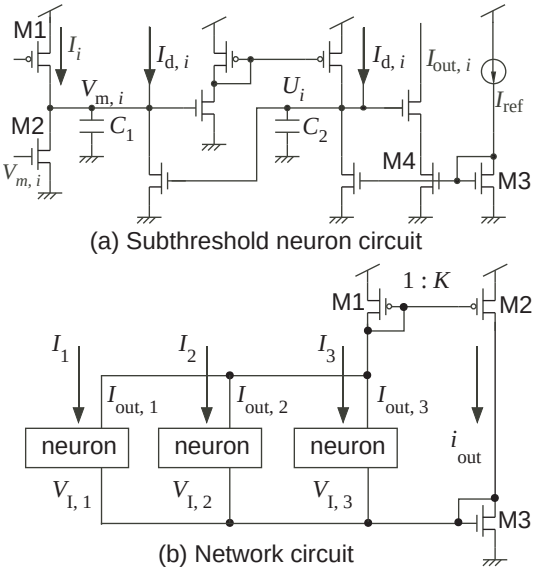

Fig. 1. (a) Subthreshold neuron circuit and (b) network circuit consisting of three noisy neuron circuits and additional circuits (M1, M2 and M3) acting as a global inhibitor

In this section, we show a possible way to handle both static and dynamic noises in analog integrated circuits by employing neuromorphic architectures. To achieve this, we employ a population model of spiking neurons that exhibits noise shaping [3]. Through circuit simulations of the network circuit, we demonstrate that the network can improve the system's signal-to-noise ratio (SNR) as a result of effectively using the static and dynamic noises.

A. Subthreshold CMOS circuits for implementing Mar's inhibitory neural network

An inhibitory network model that exhibits noise shaping with noisy elements was proposed by Mar *et al.* [3]. This network consists of N IFNs whose membrane potential is reset to random values after each firing, whereas the synaptic weights between inputs and IFNs are randomly distributed.They demonstrated that this noisy network model could improve the SNR as a result of noise shaping as observed in conventional sigma-delta-type ADCs [2].

We implemented Mar's noisy IFN using a subthreshold CMOS neuron circuit proposed by Asai *et al.* [4]. All the MOS transistors in the circuit operate in their subthreshold region, which ensures ultralow-power consumption as a whole. Therefore, it is suitable for achieving our purpose.

Figure 1(a) shows a schematic of the neuron circuit where C_1 and C_2 represent capacitances, $V_{\mathrm{m},i}$ the membrane potential of the i-th neuron circuit, U_i the refractory potential, I_i the exter-

nal input current, $I_{\mathrm{out},i}$ the quantized (spike) output current, I_{ref} the reference current for the quantization, $I_{\mathrm{d},i}$ the external fluctuation (dynamic noise), and $V_{\mathrm{I},i}$ the inhibitory input. When all the transistors are operating in their subthreshold region [5], the node equations of the circuit are given by

$$C_1 \frac{dV_{\mathrm{m},i}}{dt} = I_i - I_0 \exp(\kappa U_i / V_{\mathrm{t}}) + I_{\mathrm{d},i} \quad (1)$$

$$C_2 \frac{dU_i}{dt} = I_0 \exp(\kappa V_{\mathrm{I},i} / V_t) - I_{\mathrm{ref}} + I_{\mathrm{d},i} \quad (2)$$

where I_0 is the fabrication parameter, κ the effectiveness of the gate potential, and V_{t} a temperature dependent term. The maximum value of I_{out} is regulated by a current mirror (M3 and M4) with reference current I_{ref}.

A schematic of the network circuit is shown in Fig. 1(b). Since Mar's network model has uniform inhibitory connection strengths, we can reduce the wiring complexity from $O(N^2)$ to $O(N)$ [6] by introducing a global inhibitor, which facilitates the hardware implementation. The network circuit consists of the noisy neuron circuits and additional MOS circuits (M1, M2 and M3) implementing the global inhibitor. We employ three neurons ($N = 3$) to achieve small device sizes and minimum power consumption. Current outputs of noisy neuron circuits ($I_{\mathrm{out},i}$) are summed by M1. The summed current is mirrored by a current mirror (M1 and M2) with a mirror ratio of 1:K. Therefore, the output current (i_{out}) is given by $K \sum_{i=1}^{3} I_{\mathrm{out},i}$. Since M3 in Fig. 1(b) and M2 in Fig. 1(a) forms a current mirror, membrane potentials ($V_{\mathrm{m},i}$ for all i) are decreased when i_{out} is increased, which results in the global inhibition of all the neuron circuits.

To embed the random synaptic weights (static noises) of Mar's neural network, we introduced nonuniform input current I_i for each neuron. Instead of implementing random reset of the membrane potential of Mar's neural network, we introduced dynamic noises by random current pulses ($I_{\mathrm{d},i}$), whose inter-spike-intervals (ISIs) obey the Poisson distribution, for nodes $V_{\mathrm{m},i}$ and U_i. The oscillation phase of Mar's network is increased by resetting the membrane potential, whereas that of the proposed circuit is increased by the current pulses ($I_{\mathrm{d},i}$). Therefore, applying random current pulses to nodes $V_{\mathrm{m},i}$ and U_i is qualitatively the same as the random reset in Mar's original network.

B. Simulation results

In the following circuit simulations, we assumed 1.5-μm CMOS process (MOSIS, Vendor: AMIS). First, we simulated the neuron circuit shown in Fig. 1(a) to examine the effect of the random current pulses on the circuit as dynamic noises. We assumed that MOS transistors have the same dimension of $W/L = 1.6\mu\mathrm{m}/4\mu\mathrm{m}$, except for MOS transistors in current mirrors ($W/L = 16\mu\mathrm{m}/4\mu\mathrm{m}$). The external analog input current (I_i) and the reference current (I_{ref}) were set to 1 nA. The capacitances (C_1 and C_2) were set to 1 pF, and the inhibitory input voltage ($V_{\mathrm{I},i}$) was set to zero. The random current pulses $I_{\mathrm{d},i}$ obeying the Poisson distribution (the mean and variation $\lambda = 5000$) were generated with an amplitude of 1 nA and the pulse width of 10 μs. Figure 2 shows the time courses of membrane potentials of noiseless ($I_{\mathrm{d},i} = 0$) and noisy ($I_{\mathrm{d},i} \neq 0$) neurons. In Fig. 2(a), we observed periodic oscillation of $V_{\mathrm{m},i}$, whereas non-periodic oscillation was observed in Fig. 2(b) because the phase was randomly increased by the random current pulses ($I_{\mathrm{d},i}$). Since the neuron circuit produces spike outputs ($I_{\mathrm{out},i}$) when $V_{\mathrm{m},i}$ is suddenly decreased, the operation shown in Fig. 2(b) is equivalent to randomly resetting the membrane potential after the neuron's firing.

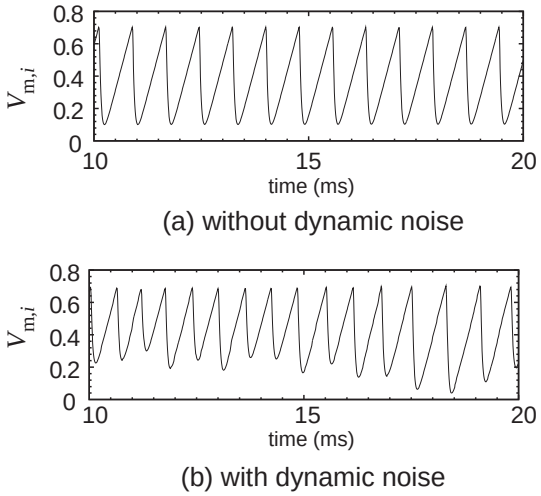

Fig. 2. Time courses of $V_{\mathrm{m},i}$ for with and without dynamic noise.

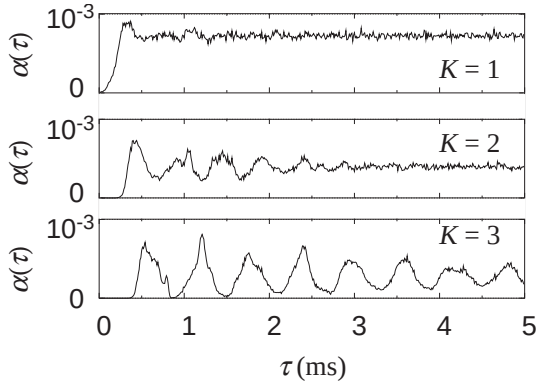

Fig. 3. Auto correlation functions of output of network circuit when inhibitory connection strength $K = 1$, 2, and 3.

Here, we describe how to determine the inhibitory connection strength K. Since a network with large values of K inhibits neurons severely, neurons with small inputs can not survive [3]. Therefore we have to choose an appropriate K for which all neurons can survive. Through our circuit simulations, we found that all neuron could survive when $K \leq 3$. To determine the best value of K, we evaluated the performance of the PDM circuit. As described above, the PDM circuit produces an output spike density that depends only on the intensity of inputs in the ideal case. In other words, the PDM circuit produces spikes periodically when the inputs is constant. Therefore, we set K so that the outputs of the circuit had high periodicity. Since the auto correlation function (ACF) can quantify the periodicity of the output, it is appropriate to determine the performance of the circuit by calculating ACFs. Because the performance of Mar's model is increases in proportion to K [3], we expected that the most appropriate value of K that is 3 or less would be 3 in order to acquire the best performance. We calculated ACFs of quantized i_{out} [$\equiv V(t)$] where i_{out} was quantized to 0 (or 1) when i_{out} was smaller (or larger) than 0.8 nA, for K = 1, 2 and 3. Figure 3 shows the results for the ACFs with $\alpha(\tau) = \langle V(t')V(t'-\tau)\rangle$. As K increased, correlation peaks appeared and apparent periodicity was observed when $K = 3$. Therefore, we set $K = 3$ where all neurons survive and the highest periodicity is observed.

Figure 4 compares the network circuit operations when $K = 0$

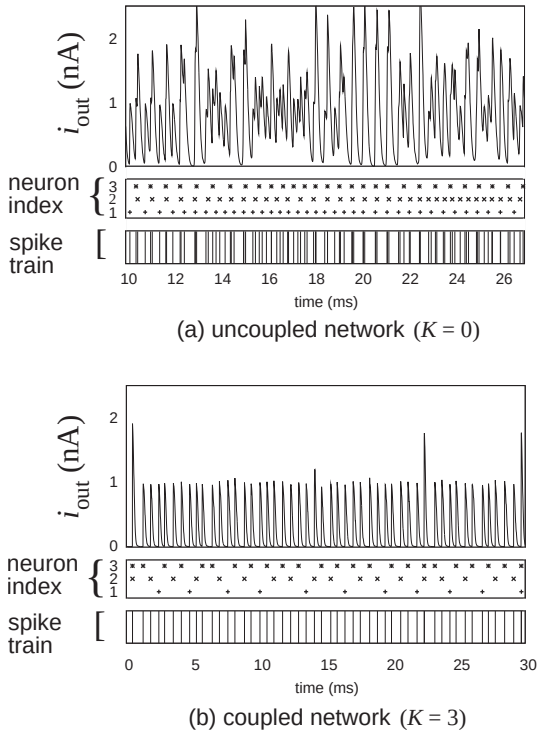

Fig. 4. Comparison of network circuit operations when $K = 0$ (uncoupled network) and $K = 3$ (coupled network).

(uncoupled) and $K = 3$ (coupled). When $K = 0$ [Fig. 4(a)], i_{out} exhibited nonperiodic oscillations. Noisy neuron circuits fired incoherently. (See raster plots in the figure. Symbols $+$, $\times$ and $*$ represent the firing events of the first, second and the third neuron circuits, respectively.) The resulting ISIs of output spike trains were random. On the other hand, when $K = 3$, i_{out} exhibited almost periodic oscillations [Fig. 4(b)]. The raster plots in the figure show significant differences between firing frequencies of three noisy neuron circuits as compared to the raster plots in Fig. 4(a). The resulting ISIs of output spike trains were almost uniform, as expected.

Figure 5 shows ISI histograms of the uncoupled ($K = 0$) and coupled ($K = 3$) network circuits where 1500 firing events were gathered with $\Delta = 0.01$ ms. When $K = 0$, we observed a Poisson-type distribution of ISIs (solid line in Fig. 5) because each neuron circuit was driven by independent noise sources and thus fired incoherently. When $K = 3$, a Gaussian-type distribution was observed (dashed line in Fig. 5). Once a neuron circuit receiving the maximum external input fires, the network is globally inhibited. After this firing, the neuron circuit operates in its refractory state. Therefore, ISIs of this neuron are higher than in the uncoupled case. Also, the neuron circuit cannot fire when the other neuron circuit receiving a smaller input than the maximum input, fires. Therefore, ISIs of output spike trains follow ISIs of a neuron receiving the maximum input, and the ISIs are averaged over the firing events of all neurons.

Figure 6 shows the PSD of the coupled ($K = 3$) and uncoupled ($K = 0$) networks with sinusoidal inputs ($I_i = I_0 + A\sin(2\pi ft)$, $I_0 = 1$ nA, $A = 50$ pA, $f = 100$ Hz) where 16 trials were averaged with a square window function. The measured SNR of the uncoupled network was 10.2 dB, while that of the coupled one was 18.1 dB, which indicated that the noise level of the coupled network was less than one tenth of that of the uncoupled network below the cutoff frequency ($< 10^3$ Hz).

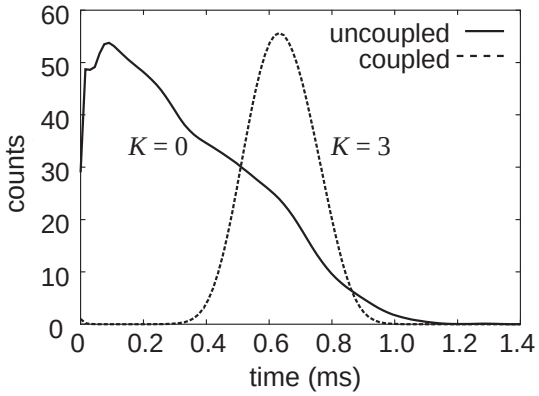

Fig. 5. ISI histograms for uncoupled ($K = 0$) and coupled ($K = 3$) networks.

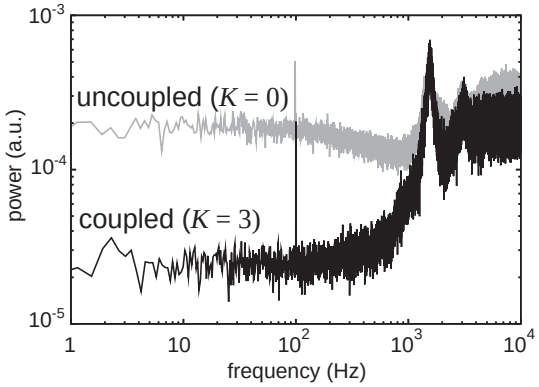

Fig. 6. Power spectra of uncoupled ($K = 0$) and coupled ($K = 3$) networks.

The external random current pulse obeying Poisson distribution is theoretically anti-correlated noise. The change in ISI distributions from the Poisson type to Gaussian type in Fig. 5 implies that the amount of noises was decreased by the effect of the global inhibition. As observed in raster plots in Fig. 4(b), individual neurons fired irregularly and thus seemed not to contribute to the signal transmission between the analog input and the digital (spike) output. Moreover, since the firing order of the neurons was also random, they seemed to fire incoherently. However, the resulting output, the sum of firing events of neurons shown at the bottom of Fig. 4(b), was almost periodic. This mechanism appeared in the resulting PSD (Fig. 6) as noise suppression, which implies that the coupled network is immune to both static and dynamic noises unlike the uncoupled network, which critically depends on the noise characteristics of individual neurons.

III. On-chip CMOS clock generators exhibiting noise-induced synchronous oscillation

Synchronous sequential circuits with global clock-distribution systems are the mainstream of implementation in present digital VLSI systems where the clock distribution is the core of synchronous digital operations. Practical clocks given through external pads are distributed to sequential circuits being synchronous to the same clocks via distributed clock networks. System clocks for synchronous digital circuits must arrive at all the registers simultaneously. In practice, time mismatches of clock arrival which are called 'clock skew' occur in LSIs [8]. The major reasons for these mismatches derive from the system clock dis-

tribution (wiring defects or asymmetric clock paths), the propagation delay of the clock chip, and the clock traces on the board. The propagation delay is dependent on the fabrication process, voltage, temperature, and loading, which makes the clock skew even more complicated. Small clock skews prevent us from increasing the clock frequency, and large skews may result in severe malfunctions. Indeed clock-skew effects on the circuit performance rise as the integration density (∼miniaturization) or the clock frequency increases.

To resolve these clock-skew issues, various technologies on clock distribution are widely used in present digital systems such as zero-skew clock distribution [9], inserting buffers for skew compensation [10] and controlling the clock-wire length [11]. In regular circuit structures, clock skews are effectively reduced by designing clock paths based on H trees (see [12] for details including statistical analysis). For large-scale complex clock networks, optimizing buffers in the clock distribution tree usually reduces clock skew. One possible way to cancel clock skew is to use asynchronous digital circuits where only local clocks are used instead of global system clocks [13]. However, the functions of these circuits currently cannot satisfy various sophisticated demands. Moreover, major LSI designers have recently started using advanced genetic algorithms in their post-manufacturing processes to calculate the required margin [14].

The present solutions for the skew problems may increase both the total length of clock distribution wires and the power consumption, as well as optimization and post-processing costs. In this paper, we propose another solution for the skew problems. Nakao *et al.* recently reported that independent neural oscillators can be synchronized by applying appropriate noises to the oscillators [7]. We here regard neural oscillators as independent clock sources on LSIs; i.e., clock sources are distributed on LSIs, and they are forced to synchronize with the addition of artificial (or natural if possible) noises. In the following sections, we show a modified neuron-based model that are suitable for hardware implementation, neuron-based clock generators for sub-RF operations (< 1 GHz), and circuit simulation results representing synchronous (or asynchronous) oscillations with (or without) external noises.

A. The Model

In the original model [7], the FitzHugh-Nagumo neuron was used to demonstrate the noise-induced synchronization between the time courses of N trials under different initial conditions. Instead we use N Wilson-Cowan oscillators in our model that are suitable for analog CMOS implementation. The dynamics are given by

$$\frac{du_i}{dt} = -u_i + f_\beta(u_i - v_i), \tag{3}$$

$$\frac{dv_i}{dt} = -v_i + f_\beta(u_i - \theta) + I(t), \tag{4}$$

where u_i and v_i represent the system variables of the i-th oscillator, θ the threshold, $I(t)$ the common temporal random impulse and $f_\beta(\cdot)$ the sigmoid function with slope β.

Figure 7 shows numerical simulation results of a single Wilson-Cowan oscillator receiving temporal random impulses given by $I(t) = \alpha \sum_j \delta(t - t_j^{(1)}) - \delta(t - t_j^{(2)})$ where $\delta(t) = \Theta(t) - \Theta(t - w)$ (Θ, w and t_j represent the step function, the pulse width and the positive random number with $t_j^{(1)} \neq t_j^{(2)}$ for all js, respectively). The system parameters were $\theta = 0.5$, $\beta = 10$, $\alpha = 0.1$, $w = 1$, and the averaged inter-spike interval of $|I(t)|$ was set at 100. We observed the limit-cycle oscillations,

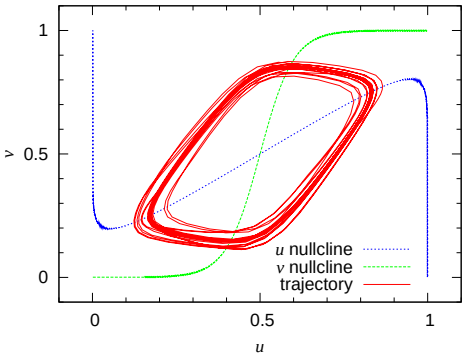

Fig. 7. Nullclines and trajectories of single Wilson-Cowan type oscillator receiving random impulses.

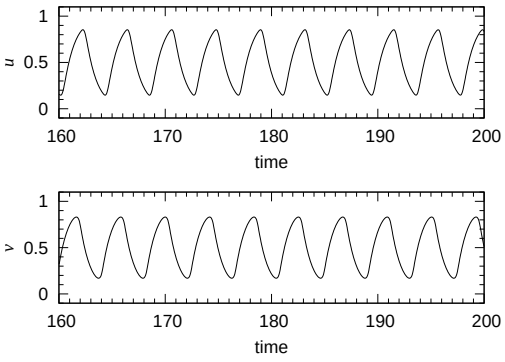

Fig. 8. Time courses of system variables of single Wilson-Cowan type oscillator receiving random impulses.

and confirmed that the trajectory was certainly fluctuated by $I(t)$. The time courses of u and v are shown in Fig. 8.

We conducted numerical simulations using 10 oscillators ($N = 10$). All the oscillators have the same parameters, and accept (or do not accept) the common random impulse $I(t)$. The initial condition of each oscillator was randomly chosen. Figure 9 shows the raster plots of 10 oscillators (vertical bars were plotted at which $u_i > 0.5$ and $du_i/dt > 0$). When the oscillators did not accept $I(t)$ ($\alpha = 0$), they exhibited independent oscillations as shown in Fig. 9(a); however, all the oscillators were synchronized when $\alpha = 0.1$ as shown in Fig. 9(b). To evaluate the degree of the synchronization, we use the following order parameter:

$$R(t) = \frac{1}{N}\left|\sum_j \exp(i\theta_j)\right|,$$

where N represents the number of oscillators, i the imaginary unit and $\theta_j = \tan^{-1}[(v_j - v^*)/(u_j - u^*)]$ ((u^*, v^*) represents the fixed point of the oscillator). When all the oscillator are synchronized, $R(t)$ equals 1 because of the uniform θ_js, while $R(t)$ is less than 1 if the oscillators are not synchronized. Figure 10 shows the time courses of the order parameter values. When $\alpha = 0$, $R(t)$ was unstable and was always less than 1 [Fig. 10(a)], whereas $R(t)$ remained at 1 after it became stable at $t \approx 2000$ when $\alpha = 0.1$ [Fig. 10(b)]. These results indicate that if we implemented these oscillators as clock generators on CMOS LSIs, applying common random pulses to the oscillators could synchronize them.

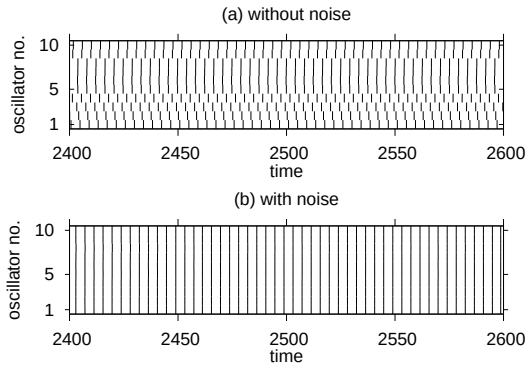

Fig. 9. Raster plots of 10 oscillators. (a) independent oscillations without random impulses, (b) synchronous oscillations with random impulses.

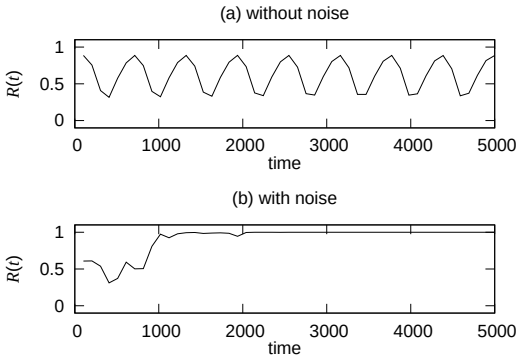

Fig. 10. Time courses of order parameter values (a) without random impulses and (b) with random impulses.

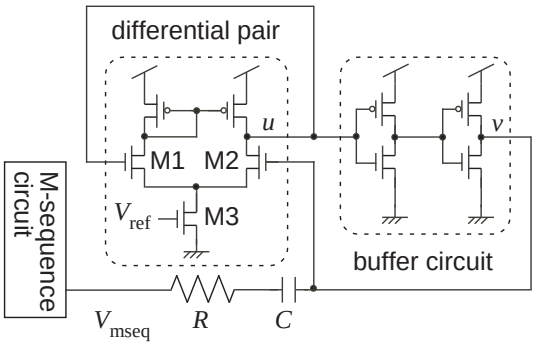

Fig. 11. Wilson-Cowan circuit for sub-RF operations.

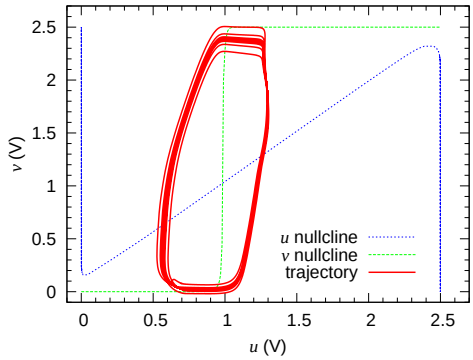

Fig. 12. Nullclines and trajectories of oscillator circuit receiving pseudo-random impulse.

B. The circuit and simulation results

We designed a Wilson-Cowan oscillator circuit for sub-RF operations (Fig. 11). The circuit consists of a differential pair (M1 to M3) and a buffer circuit composed of two standard inverters. In the following simulations, we used TSMC's 0.25-μm CMOS parameters with $W/L = 0.36$ μm / 0.24 μm except for M3's channel length ($L = 2.4$ μm). Pseudo-random sequences ($V_{\rm mseq}$) were generated using a 4-bit M-sequence circuit, and were distributed to the circuit through a RC filter. The supply voltage was fixed at 2.5 V.

Figure 12 shows SPICE results of the nullclines and trajectories receiving random impulses ($C = 10$ fF, $R = 100$ kΩ, the clock frequency of the M-sequence circuit was 50 MHz, which resulted in a 300-ns pseudo-random sequence). Time courses of u and v are shown in Fig. 13. We observed qualitatively-equivalent nullclines and trajectories to those of the Wilcon-Cowan oscillators. We confirmed the limit-cycle oscillations where the trajectory was effectively fluctuated by the M-sequence circuit with the RC filter. The oscillation frequency was about 1 GHz when the reference voltage $V_{\rm ref}$ was set at 1 V. Figure 14 shows the raster plots of 10 oscillator circuits (vertical bars were plotted at which $v_i > 1.25$ V and $dv_i/dt > 0$). All the circuits exhibited independent oscillations when random sequence $V_{\rm mseq}$ was not given to them [Fig. 14(a)], whereas they exhibited complete synchronization when $V_{\rm mseq}$ was given [Fig. 14(b)]. Time courses of the order parameter values were shown in Fig. 15. When random impulse was not given to the circuit, $R(t)$ was not stable and was always less than 1 [Fig. 15(a)], while $R(t)$ remained at 1 after it became stable at $t \approx 700$ μs when random impulse was given [Fig. 15(b)].

Our results indicate that if we distributed these circuits as ubiquitous clock sources on CMOS LSIs, they could be synchronized when common random impulses were given to the circuits. Although this may cancel out the present clock skew problems, device mismatches between the clock sources may prevent the sources from complete synchronization. Therefore, we investigated the device-mismatch dependence of the proposed circuits. For our distributing purposes, local mismatches in a single oscillator circuit would be negligible; i.e., mismatches in a differential pair (M1 and M2) and a current mirror. Mismatches in inverters corresponding to threshold θ in Wilson-Cowan model would also be negligible because they only shift the fixed point, and do not vastly change the oscillation frequency. However, mismatches of M3 between the oscillators may drastically change each oscillator's intrinsic frequency. Therefore, we distributed threshold voltages of M3s of all the oscillators. Zero-bias threshold voltages (VTO) of M3s were randomly chosen from the Gaussian distribution (mean: 0.37 V and standard deviation: σ). Figure 16 shows the dependence of averaged order-parameter values $\langle R(t) \rangle$ (from 0 to 1 μs) on σ. We generated 10 random VTO sets for each σ, and plotted the error bars and the mean values in the figure. We confirmed that $\langle R(t) \rangle$ was gradually decreased when σ was increased.

IV. High-fidelity pulse-density modulation with noisy neuromorphic circuits based on a model of vestibulo-ocular reflex

Here we explore possible ways to construct an electrical circuit that can perform high-speed information processing with slow devices. Regarding this point, neural networks seem to

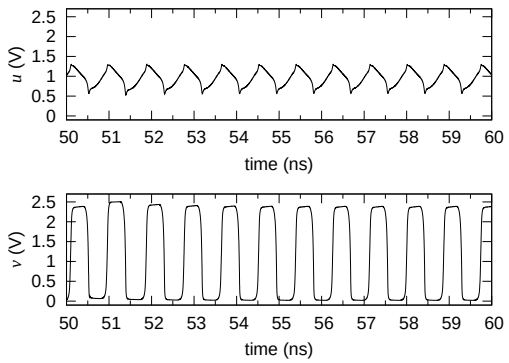

Fig. 13. Time courses of system variables of oscillator circuit receiving pseudo-random impulses.

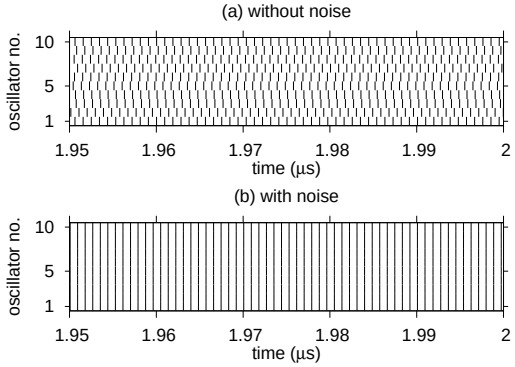

Fig. 14. Raster plots of 10 oscillator circuits. (a) independent oscillations without random impulses, (b) synchronous oscillations with random impulses.

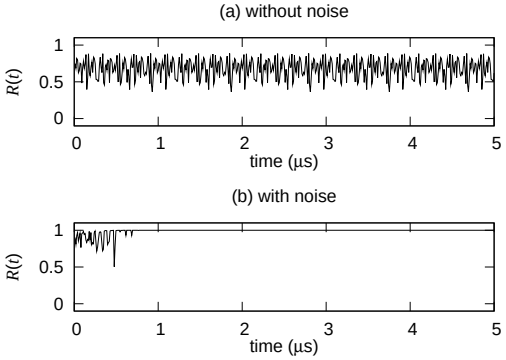

Fig. 15. Time courses of order parameter values (a) without random impulses and (b) with random impulses.

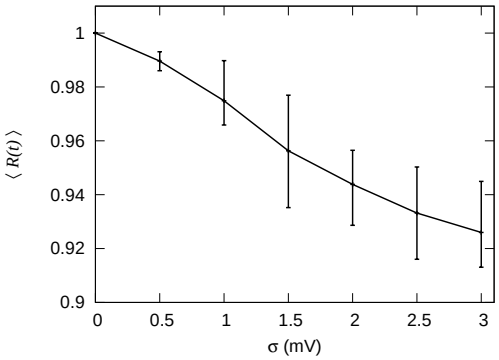

Fig. 16. Synchrony dependence on parameter mismatch.

be a possible choice because they are considered to perform high-speed parallel information processing with neuron elements which are relatively slower than CMOS transistors. In recent study, Hospedales *et al.* reported that a neural network with temporal noises and spatial noises in neurons that was used to perform "vestibulo-ocular reflex" (VOR) could conduct a temporal signal whose frequency was higher than operation frequency of a single neuron in networks [15]. VOR stabilizes the visual field by moving the eyeballs in such a way that compensates for rotations of the head. They reported that this function could be achieved by using temporal and spatial noises of neurons. Figure 17 shows a simple schematic of the model. The four neurons ($N = 4$) represented by the open circles are connected in parallel. All the neurons accept common input and generate spike output i (i: neuron number). The output of the network is given by summing of outputs of all the neurons. When no noises are applied to this network, all the neurons generate spike output at the same time (phase). However, when they are affected by temporal noises ξ_i and spatial noises δ_i, they no longer can generate spike output at the same time. It represents that the network shows asynchronous firing and it can thus respond to relatively faster input signal than a single neuron.

The operation frequency in electrical circuits of a single device is limited by several conditions that derive from physical limitations. Electrical circuits are often limited by power consumption or chip area size especially in mobile appliances or sensor appliances. Information processing done by the brain is considered to have an energy-efficient structure. The architecture observed in the brain may provide possible solutions to electrical engineering. Further more, electrical-circuit engineers often try to reduce or eliminate the effects of noises and device mismatches of transistors because these effects degrade circuit characteristics and they even cause erroneous circuit operation. Typical circuit designs to reduce these effects often require additional transistors and larger transistors (= larger chips and greater power consumption), which makes it more difficult to meet the specification. Here, by implementing Hospedales et al.'s model in electrical circuits, noises and device mismatches in these circuits could be utilized to improve operations while group of slow devices could achieve faster operation. We constructed a simple neural-network circuit to confirm the improvements in fidelity and we then demonstrate that the operation frequency of a noisy network circuit is higher than that of a noiseless network circuit.

A. CMOS pulse-density modulator implementing neural network model of VOR

Based on the results obtained by Hospedales *et al.* [15], we developed a network circuit consisting of multiple MOS neuron circuits. Figure 18 shows a schematic of an i-th neuron circuit based on the Wilson-Cowan oscillator model [16]. The u_i and v_i represent system variables of the i-th oscillator, V_b the bias voltage, C_1 and $C_{2,i}$ the capacitance, and the $V_{\mathrm{mseq},i}$ the pseudo noise voltage generated by a 4-bit M-sequence circuit. The $V_{\mathrm{mseq},i}$ fluctuates the trajectories occurred in the circuit so that phase advance or delay of the oscillator occurs. The oscillator circuit accepts pulsed input voltage V_in and generates a spike event (v_i) when V_in increases. After a spike is gener-

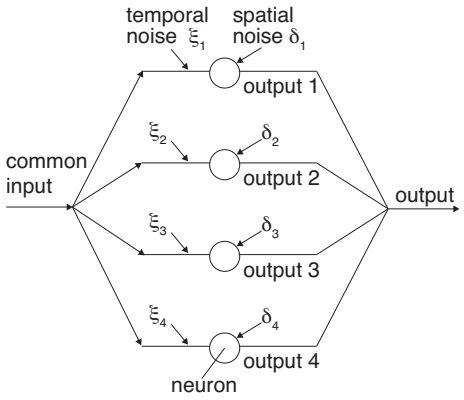

Fig. 17. Neural network model of VOR

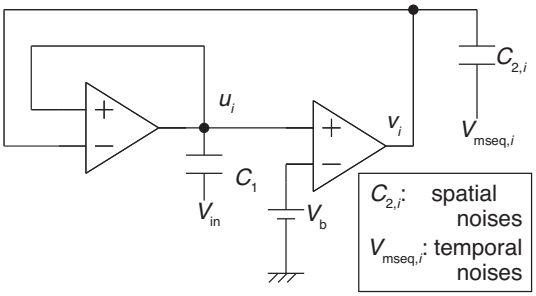

Fig. 18. Wilson-Cowan neuron circuit

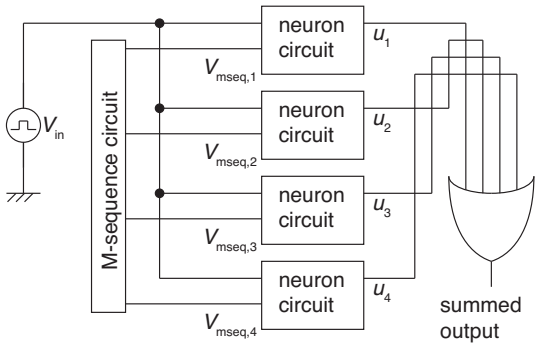

Fig. 19. Neural network circuit

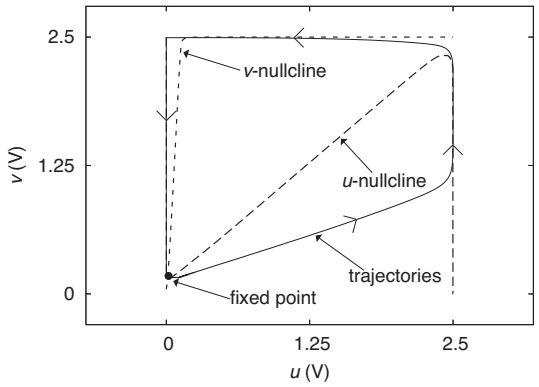

Fig. 20. Trajectories and nullclines for u and v of single neuron circuit

ated, the circuit can hardly generates s spike even if an input signal is applied for a certain period. This period is called the "refractory period" in biology. After this period, it can generate spike events. This means that when the input frequency is higher than a certain threshold, the circuit can not correctly responds to the input. The length of the refractory period is mainly determined by a capacitance $C_{2,i}$. Figure 19 has a schematic of a network circuit. Four neuron circuits were used for our preliminary research ($N = 4$). The spatial noises in the model can be mimicked by setting $C_{2,i}$ to different values. Consequently, each neuron circuit has a slightly different refractory period and has a slightly different limitations in intrinsic frequency. These neurons accept identical (correlated) pulsed signal V_{in} and uncorrelated pulsed signal $V_{\mathrm{mseq},i}$. Because the noises signal $V_{\mathrm{mseq},i}$ drastically change phases by applying fluctuations to v_i, no firing events by neurons occur with the same timing although common input is applied to all the neurons. This means that the probability of the network firing remains high when noises are applied. The entire output is expressed by the logical summing of all neurons' output events with the OR logic circuit.

B. Simulation results

Figure 20 shows the nullclines and trajectories for a noiseless ($V_{\mathrm{mseq},i} = 0$ V) single ($N = 1$) neuron circuit. In simulations of the simgle neuron circuit, C_1 was 100 fF, $C_{2,1}$ was 300 fF, V_{dd} was 2.5 V, and the clock frequency of the M-sequence circuit was set to 0.5 kHz.V_{b} was set to 0.12 V so that the neuron circuit would stay stable if input signal V_{in} did not contain a temporal signal. We confirmed the excitatory operation after pulse input was applied as shown in Fig. 20. Figure 21 shows simulated responses of a noiseless oscillator ($V_{\mathrm{mseq}} = 0$) to variable input-pulse frequencies (f_{in}). When f_{in} was 0.4 kHz [Fig. 21 (a)], the neuron could conduct input pulses and generates spike output in response to the rise time of input pulses. However, when f_{in} was 0.5 kHz [Fig. 21 (b)], the neuron could not conduct these input pulses and the neuron generated spike events once every two input pulses. We confirmed that the single neuron circuit could responds to temporal signals whose frequencies is lower than 0.4–0.5 kHz. To visualize the relationship between pulse input frequency f_{in} and the spike output frequency f_{out}, we plotted the dependence of f_{out} on f_{in} in Fig. 22. The open squares represent the simulation results and the solid line is an approximated curve for these data. As seen from the figure, the circuit could conduct input whose frequencies were 0–0.4 kHz while it could not conduct input whose frequencies were over 0.4 kHz. This limitation depended on capacitance $C_{2,i}$.

We will now discuss what the effect noises had in our network circuit. We conducted simulation with and without noises. No noises meant that none of the four neuron circuits accepted temporal noises given by $V_{\mathrm{mseq},i}$ and each capacitance $C_{2,i}$ had the same value (300 fF). Applying noises meant that all the neuron circuits accepted individual temporal noises ($V_{\mathrm{mseq},i}$) and the value of $C_{2,1}, C_{2,2}, C_{2,3}$, and $C_{2,4}$ were set to correspond to 280, 290, 300, and 310 fF. Raster plots and output of the network circuit in Fig. 23 indicate the performance of the circuit without noises [Fig. 23 (b)] and with noises [Fig. 23 (c)]. We set f_{in} to 1.2 kHz which is faster than operation frequency of a single neuron circuit (0.4 kHz). Figure 23 (a) shows the input signal. The symbols $+, \times, *$, and $\square$ in Fig. 23 correspond to firing events for neurons 1, 2, 3, and 4, and the vertical line represents the firing events of the whole network circuit. When no noises were applied, the four circuits had exactly the same characteristics; thus all their outputs is identical as shown in Fig. 23. This meant that the output of the four neurons had the same value

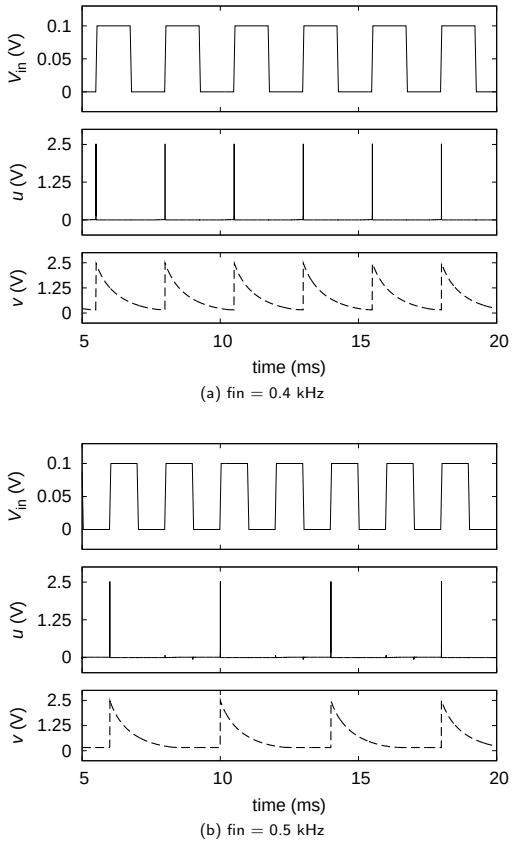

Fig. 21. Simulated response of single neuron

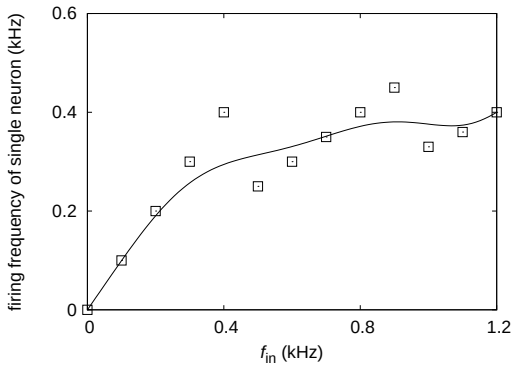

Fig. 22. Dependency of firing frequency of single neuron on input frequency

as the output of a single neuron. This also meant that even if more neurons were employed the performance of the network circuit would not be improved. When noises were applied to neurons, their individual response to common input was different due to noises because they dynamically changed the state of each neuron. The outputs of a single neuron are not periodic and seem to be random. However, output could express an input signal. The output of a network circuit with noises has an irregular signal that is caused by noises.

We showed that a noisy circuit surpasses a noiseless circuit in its response to an input signal. Dependence of $f_{\rm out}$ on $f_{\rm in}$ plotted in Fig. 24 demonstrate the performance. The open squares plot results for the circuit without noises and the filled circles show results for the circuit with noises in Fig. 24. The solid

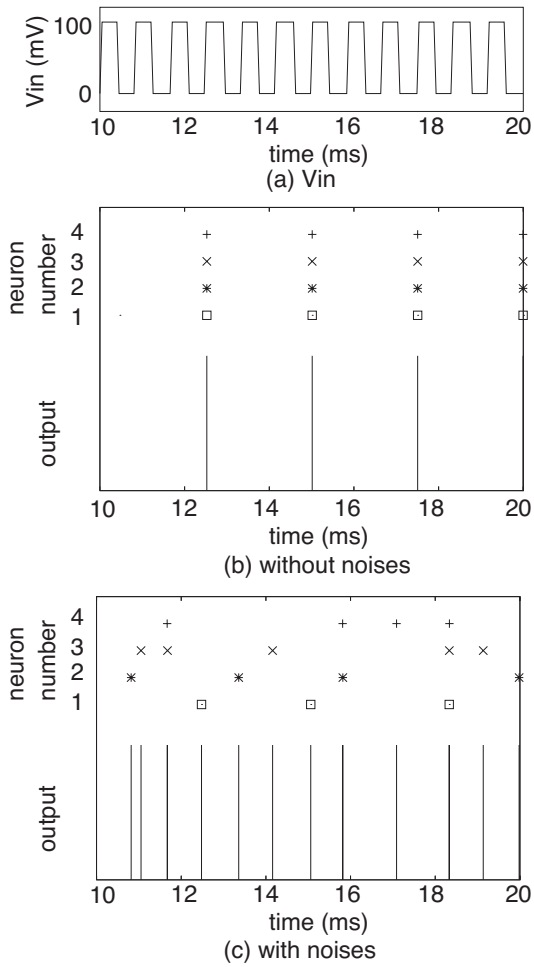

Fig. 23. Raster plots and output event of network circuit

black line represents where $f_{\rm in} = f_{\rm out}$. The noiseless circuit had the same characteristics as shown in Fig. 22. This circuit could respond to 0.4 kHz, which is the upper limit frequency of a single neuron circuit, and it could not respond to frequencies that were higher than the limit frequency of a single neuron. When noises were applied to the circuit, the same characteristics were qualitatively confirmed with the model. When $f_{\rm in}$ was low $f_{\rm out}$ was higher and almost same value (0.5 kHz). When $f_{\rm out}$ was high $f_{\rm out}$ was linear to $f_{\rm in}$. It was difficult to achieve these characteristics without noises. Applying random initial conditions may achieve the same characteristics in the noiseless circuit because random initial conditions give phase delay and firing events occur randomly for each neuron. However, even if random initial conditions were applied their phases were synchronized by a common input signal whose frequency and amplitude do not have a fixed value.

V. Summary

First, we demonstrated a possible way to develop a one-bit analog-to-digital converter in a noisy environment. We proposed a network circuit inspired by neuromorphic architectures to subtly utilize static and dynamic noises in VLSIs. We employed a population model of spiking neurons [3]. This model has a network using inhibitory coupling that exhibits noise shaping. We implemented this model with subthreshold MOS circuits to actively employ noise. The static and dynamic noise ap-

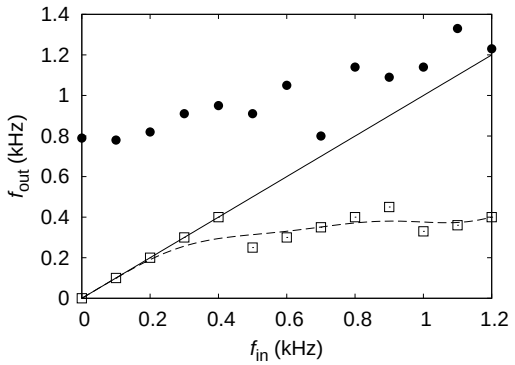

Fig. 24. Dependence of $f_{\rm out}$ on $f_{\rm in}$

plied to the circuit for noise shaping were obtained from device mismatches of current sources and externally applied random (Poisson) spikes, respectively. A coupled network produced a Gaussian-like distribution of inter-spike intervals (ISIs), while an uncoupled one had a broad distribution of ISIs. Through circuit simulations we confirmed that the signal-to-noise ratio of a coupled network was improved by 7.9 dB compared with that of an uncoupled one as a result of noise shaping.

Second, we showed CMOS sub-RF oscillators that could be synchronized using common random impulses, based on a theory in [7]. We proposed a modified Wilson-Cowan model for implementing FitzHugh-Nagmo oscillators. We confirmed that the synchronization properties of the modified model were qualitatively equivalent to those of the original model. We then designed sub-RF oscillator circuits based on the modified model. Through circuit simulations, we demonstrated that the circuits exhibited the same synchronization properties as in the original and modified models. For our clock-distributing purposes, we investigated the synchrony dependence on device mismatches between the distributed oscillator circuits. The result showed that the synchrony was gradually decreased when variance of the mismatch was linearly increased, which indicated that our 'ubiquitous' clock sources with small device mismatches would be synchronized by optimizing our parameter sets.

Finally, we introduced a neuromorphic circuit with high fidelity in its output spike train based on the Vestibulo-Ocular Reflex (VOR) model. We constructed a network circuit consisting of neuron circuits, an M-sequence circuit, and an OR logic circuit. We confirmed that a single neuron circuit could operate up to 0.4 kHz and it operated incorrectly over 0.4 kHz. When four neurons were used in simulations, the network without noises had the same characteristics while the network with noises had higher performance than that without noises. The noisy network could operate correctly at 1.2 kHz and we confirmed that fidelity could be increased by noises. We were forced to limit the operation frequency of the neuron circuit that we introduced in this report forced to a certain value due to the size of capacitance in the circuit. We plan to use a subthreshold CMOS circuit that allows an ultra-low power circuit even though device mismatches strongly degrades circuit characteristics.

We have recently extended our noise-driven CMOS circuits to "single-electron circuits" that are much more sensitive to both external and internal (thermal) noises, e.g., single-electron neural network for synchrony detection [17], stochastic resonance in single-electron circuits [18], [19], single-electron circuits performing dendritic pattern formation with nature-inspired cellular automata [20], single-electron image processing architectures for edge detection [21] and motion detection [22], a noise-shaping single-electron pulse-density modulator [23], and so on.

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