Threshold-logic systems consisting of subthreshold CMOS circuits

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Abstract: We propose a threshold-logic gate device consisting of subthreshold MOSFET circuits. The device performs threshold-logic operation, using a technique of current addition and subtraction. To examine the operation of the device, we designed sample subsystems, adders, based on majority logic and confirmed their operation by computer simulation. The device has a simple structure and operates at low power dissipation, so it is suitable for constructing cell-based, parallel processing LSIs such as cellular automaton and neural network LSIs.

1. Introduction

Threshold logic is a way of digital processing and more functional than conventional AND-OR Boolean logic. To construct LSIs based on threshold logic, we must develop gate devices for threshold-logic operation that are compatible with silicon technology. This paper proposes one such device, a threshold logic gate consisting of MOSFET circuits.

Threshold logic is a way of implementing digital operations in a manner different from that of Boolean logic. Instead of using Boolean logic operators (AND, OR, and their complements), threshold logic represents and manipulates digital functions on the basis of *threshold comparison*. The logic process of threshold logic is much more sophisticated than that of Boolean logic; consequently, threshold logic is more powerful for implementing a given digital function with a smaller number of logic gates. Besides, threshold logic is a basis of several functional processing methods such as the cellular automaton, the neural network, and the holonic processing.

In this paper, we propose a method of constructing gate devices for threshold logic. Section 2 outlines the unit function required for threshold logic and presents a method of implementing the function using a technique of current addition and subtraction. Section 3 presents a gate device that implements the unit function. The device consists of a MOSFET circuit operated in the subthreshold region, i.e., the region where the gate-source voltage is small and drain-source current is in a range of 1-100 nA. The transfer characteristics of the device is shown by computer simulation. Section 4 describes the design of simple subsystems, adders, that consist of the gate devices. The simulated operation of these subsystems is also described.

2. Implementing the function of threshold logic

(*Unit function of threshold logic*)

The unit function of threshold logic is determining the output logic value on the basis of threshold comparison. The logic element, a threshold-logic gate, has a number of binary inputs and a binary output. It produces an output of 1 if the sum of inputs is larger than a threshold value, and produces an output of 0 if the sum is smaller than the threshold. The function of a five-input gate is shown in Fig. 1 for various values of threshold. When, for instance, the threshold is 3.5, the output is 0 for inputs 1, 1, 0, 0, 1, and the output is 1 for inputs 1, 1, 0, 1, 1. (For further details on threshold logic, see Ref. [1]) Any digital function can be implemented using a combination of threshold gates and inverters. If a gate has odd number n of inputs and the threshold is set to $n/2$, the gate is called a majority gate because its

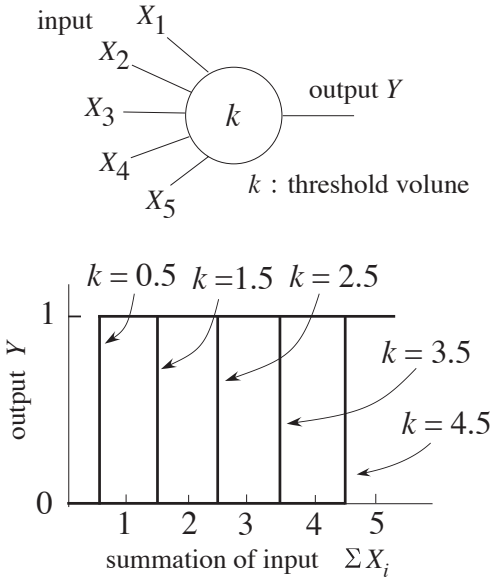

Fig.1: Symbol for threshold-logic gate and its function with a five-binary-input and a binary output for various values of threshold *k*.

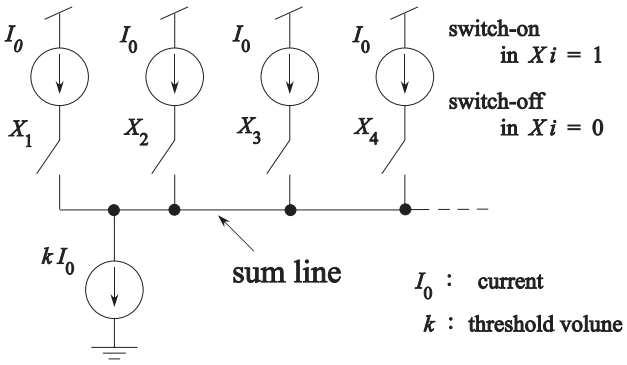

Fig.2: Threshold logic circuit on the basis of current addition-subtraction technique.

output is determined with majority vote of 1-0 inputs. Three-input majority gates suffice for the construction of any logic system.

(*Implementing the unit function*)

To implement such threshold logic operation, we developed a gate circuit on the basis of current addition-subtraction technique. The concept of the circuit is illustrated in Fig. 2. The circuit consists of two subcircuits: a threshold current source kI_0 and

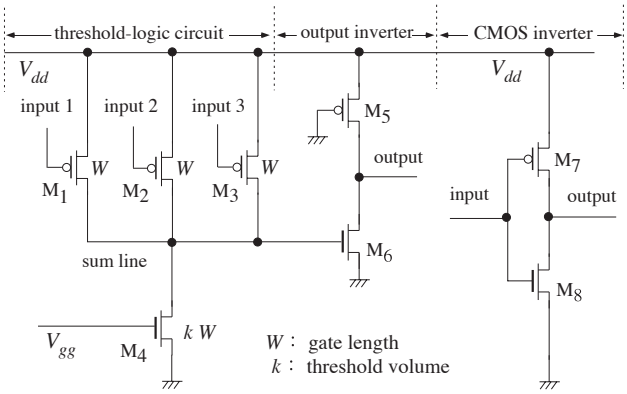

Fig.3: A threshold-logic gate consisting of CMOS circuit.CMOS inverter is also shown.

input current sources I_0 with switches controlled by binary input signals X_i (the switch is on for X_i = 1). The threshold current source drains current kI_0 from the sum line, and each input current source injects current I_0 into the sum line. The net current injected to the sum line is $(\sum Xi - k)I_0$.

The circuit accepts 1-0 binary inputs *Xi* and compares the number of 1-inputs with threshold value *k* to produce the corresponding output voltage. If the number of 1-inputs is larger than *k*, the net current injected to the sum-line is positive and, consequently, the sum-line voltage will rise to a 1 state; otherwise the net current is negative and the sum-line voltage will fall to 0 state.

3. Constructing a threshold-logic gate circuit

(*Gate circuit*)

The gate circuit (M1-M6) we propose is illustrated in Fig. 3, with an example of a three-input configuration (a CMOS inverter M7-M8 is also shown). It consists of input transistors M1-M3 with a gate width of *W*, threshold-current transistor M4 with a gate width of *kW* (*k*; threshold value) and an output inverter M5-M6. Bias voltages V_{dd} and V_{gg} are set to appropriate values so that, when the input voltage is 0, the current through each of M1-M3 will be 1/*k* of the

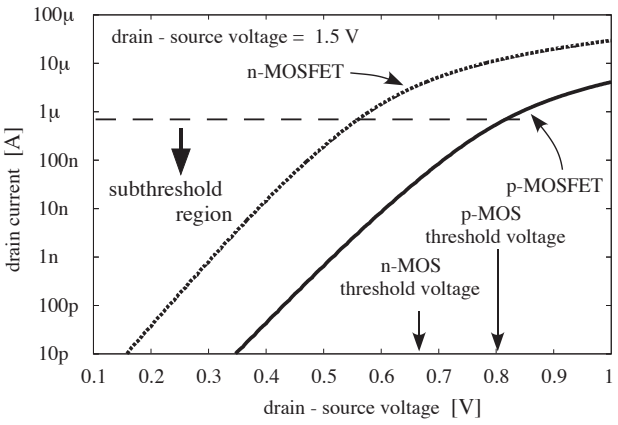

Fig.4: Transfer characteristic of nMOS and pMOS transistors. Transistor sizes were set to 1 μm/0.35 μm.

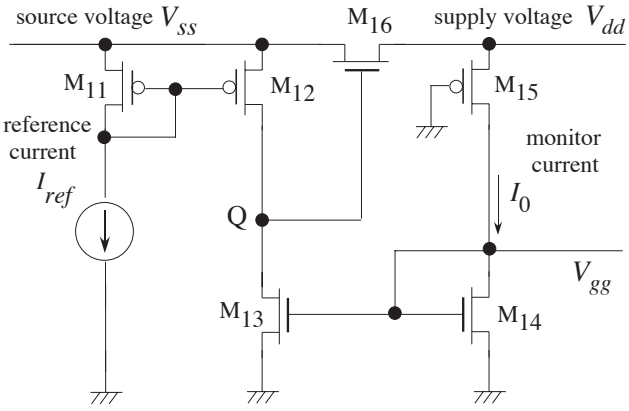

Fig.5: Power supply for subthreshold logic gates (n-MOS type circuit implementation).

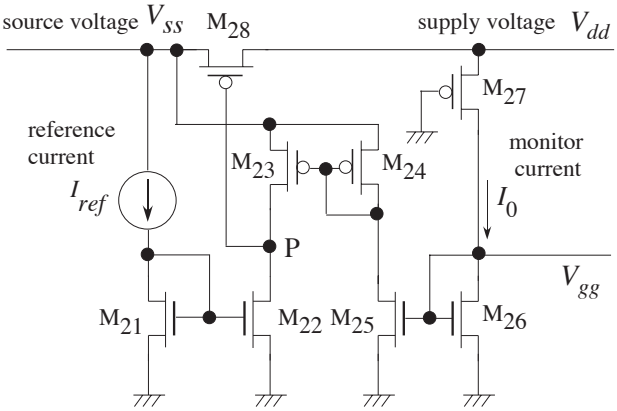

Fig.6: Modified power supply for subthreshold logic gates capable of low power supply voltage operation (p-MOS type circuit implementation).

current through M4; this can be performed by a power supply circuit shown later in Fig. 5 and Fig. 6.

The operation of the gate circuit is as follows. If the number of 1-inputs (or inputs with voltage V_{dd}) for M1-M3 is smaller than threshold k, the net current injected to the sum line is positive. This raises the voltage of the sum line to a high value, so the output of inverter M5-M6 falls to 0 (logic 0). In contrast, if the number of 1-inputs is larger than k, the net current for the sum line is negative; consequently, the voltage of the sum line falls to a low value, and the output of the inverter rises to V_{dd} (logic 1).

Our threshold logic gate uses a current flow for logic operation, thereby producing power dissipation even in a static state; this would be inevitable generally in threshold gate devices and other analog-like logic devices. To reduce power dissipation, we operated the gate circuit in the subthreshold region of MOSFETs.

The subthreshold region is a region where the gate-source voltage of a MOSFET is smaller than the threshold voltage of the MOSFET (see [2] for details of the subthreshold operation of MOSFETs). Figure 4 shows the transfer characteristics of nMOS and pMOS transistors we used to design the gate circuits (0.35 μm CMOS devices). In this example, the a region where current is 1 μA or less is the subthreshold region. In our gate circuit, we operate all MOSFETs in a current range of 1-100nA. This can be performed by setting bias voltages V_{dd} and V_{gg} for the gate to appropriate values. For this purpose, we designed a power supply circuit described in the next section.

(*Power supply for the gates*)

An example of power supply circuit for subthreshold logic gates is depicted in Fig. 5 [3]. An external voltage source V_{ss} is converted to a lower voltage V_{dd} by transistor M16 to make a power supply voltage for load circuits. Transistors M14 and M15 monitor a current I_0 and generate voltages V_{dd} and V_{gg}

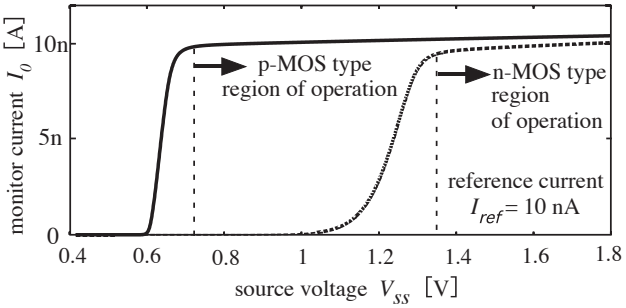

Fig.7: Transfer characteristics of the power supply circuits.

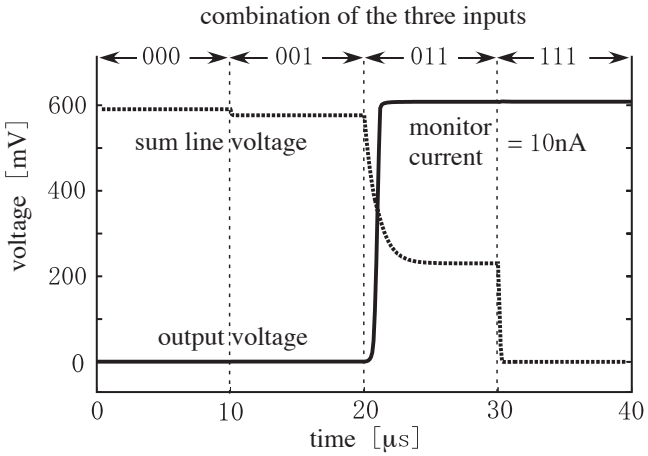

Fig.8: Simulated results of the sum-line voltage and output voltage in the majority decision gate.

for the threshold logic gates. The voltages ---V_{dd} for PMOS and V_{gg} for NMOS--- are controlled by a reference current I_{ref}, and are generated so that same current with reference current I_{ref} flows in MOSFETs in the load circuit. The circuit requires the reference current I_{ref}, and the reference current in [4] can be used for our purpose. In the following, the operation of the power supply circuit is described in more detail.

The reference current I_{ref} is injected to gate node Q of M16 through current mirror M11-M12, and a current I_0 is drained from node Q through current mirror M13-M14. If monitor current I_0 is smaller than reference current I_{ref}, the circuit operates so that the current I_0 equals to I_{ref}. This is performed through a negative feedback operation: $I_0 < I_{ref} \rightarrow$ increasing node voltage Q $\rightarrow$ decreasing on-resistance in M16 $\rightarrow$ increasing supply voltage $V_{dd} \rightarrow$ increasing monitor current $I_0 \rightarrow I_0 = I_{ref}$. And if a monitor current I_0 is larger than reference current I_{ref}, the circuit operates in a similar way of the negative feedback operation and then monitor current I_0 equals to reference current I_{ref}. The power supply circuit is stable in frequency response, but it needs to pay an attention to the reduction of external source voltage V_{ss}. This is because required voltage at the node Q is limited to the sum of voltages V_{thn} and V_{dd}. Therefore, the circuit cannot operate correctly if external voltage V_{ss} is smaller than the sum of voltages V_{dd} and V_{thn} ($V_{ss} < V_{dd} + V_{thn}$). For example, in our technology used in this work, threshold voltage of NMOS transistor is about 0.6 V, and then if monitor current I_0 is designed to 10 nA, internal supply voltage V_{dd} should be about 0.6-0.7 V. Therefore, the external source voltage V_{ss} should be more than 1.3 V as shown Fig. 7. When a button-type manganese battery cell with a nominal voltage of 1.5V is used as an external source voltage, voltage margin for a stable operation is quite small in this circuit configuration.

This problem can be solved by using PMOS type power supply circuit as shown in Fig. 6. PMOS transistor M28 is used instead of an NMOS transistor M16. The circuit operation is the same as NMOS type power supply circuit. In the circuit, the gate-source voltage of M28 should be more than threshold voltage V_{thp}. On the contrary to the NMOS circuit, node voltage P can be made low voltage, almost 0V nearly. So the external source voltage V_{ss} should be more than threshold voltage of PMOS V_{thp}. The transfer functions of each supply circuit with external supply voltage are depicted in Fig. 7. PMOS type supply circuit can work correctly with lower voltage at 0.7 V. For the stable operation, we add the compensation capacitor between gate and source node of transistor M28.

(*Transfer characteristic of the gate*)

A majority decision gate of 3-inputs can be constructed by setting threshold value at 1.5 as shown in Fig. 8 (k = 3/2). Figure 8 shows simulation results of the logic operation. In this simulation, all of

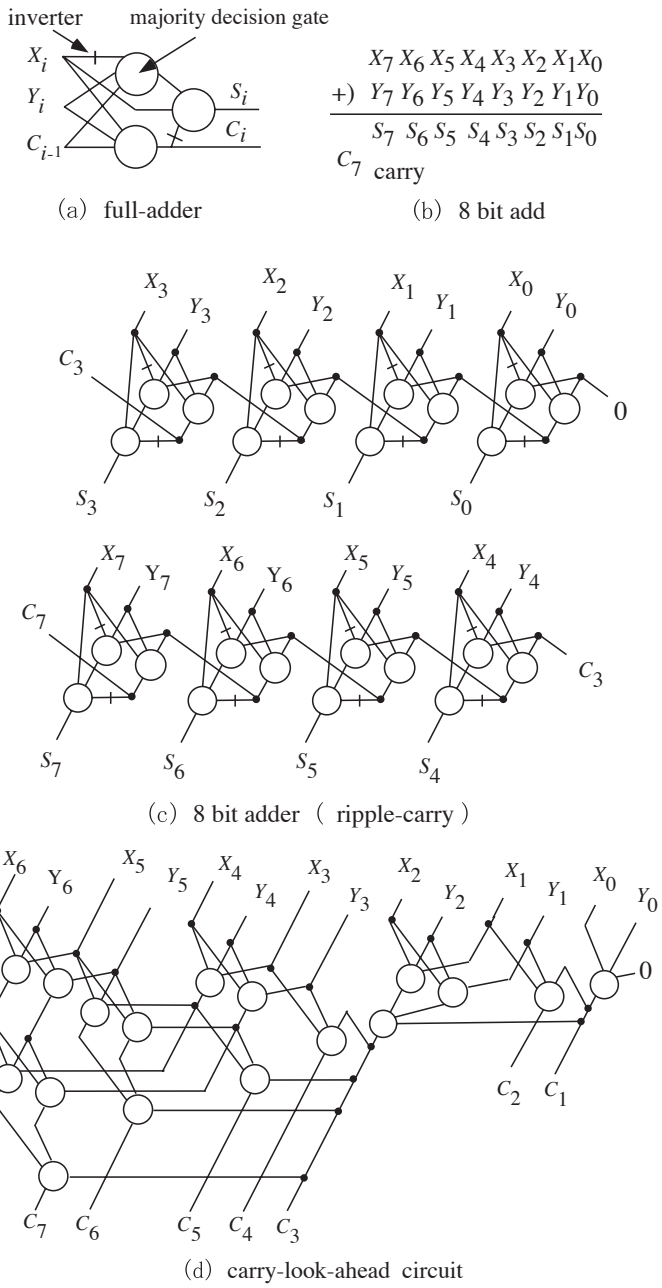

Fig.9: Schematics of (a) Full-adder circuit consisting of majority decision gate and inverters, (b) 8 bit adder operation, (c) ripple-carry(RC) adder and (d) a carry-look-ahead circuit.

MOSFET's aspect ratios were set to W/L＝1 μm/0.35 μm except for M24. The aspect ratio of transistor M24 was set to W/L＝1.5 μm/0.35 μm. The number of "1" inputs were increasing with time in this simulation. In this example, supply voltages were generated in such a way that monitor current was I_0 = 10 nA. The ganerated voltages of V_{dd} and V_{gg} were 600 mV and 390 mV, respectively. If two inputs became V_{dd} (logic "1"), voltage of sum-line falls. The inverter outputs V_{dd} (logic "1"). The circuit shows a majority decision operation. The maximum current dissipation was 28 nA, at which two inputs were 0.

When two inputs were "1", the voltage of the sum-line must be 0 because current drained from a sum-line is larger than injected current. But, the voltage of sum-line was about 200 mV. This can be understood as follows. When the number of 1-inputs is slightly larger than the threshold value, the current drained from the sum-line is larger than injected current, and then the voltage of the sum-line will decrease. However, because of the channel length modulation effects of the transistors, the drained current by nMOS transistor M4 and the injected current by input pMOS transistor were smaller and larger than their ideal current level, respectively. And therefore, injected current and drained current were balanced at this voltage. However, because the voltage of sum-line is always lower than the inverting threshold voltage of output inverter, this increase of the sum-line voltage affects no influence on the threshold logic operation.

4. Adders consisting of threshold logic gates

To confirm the operation of the gate, we design a full adder circuit by using the majority decision gate, and developed an 8 bit adder circuit by combining with CMOS inverter. The circuits are illustrated on Fig. 9.

Figure 9 (a) shows the full-adder circuit consisting of majority decision gates and inverters. The output of the sum S_i becomes "1" when the number of "1" inputs within 3-input of X_i Y_i C_{i-1} is 1 or 3 (odd parity). The carry C_i becomes "1" when the number of "1" inputs is more than 2 (majority decision). This operation can be performed by 3 majority decision gates and 2 inverters. Figure 9 (b)

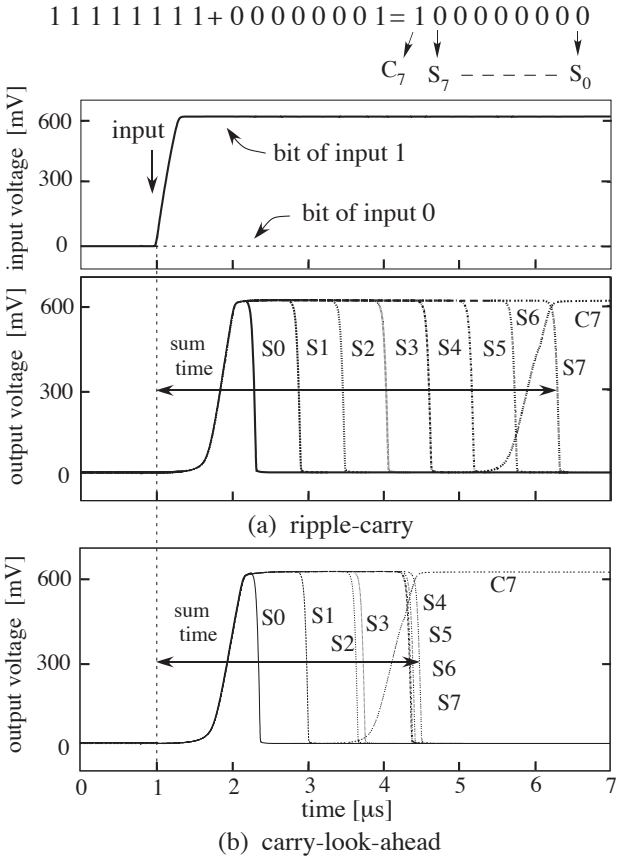

Fig.10 : Operations of 8 bit adders. Simulated waveforms of input, output of RC adder, and that of CLA adder, respectively.

shows 8 bit adder operation we designed. Figure 9 (c) and (d) show an 8 bit ripple carry (RC) adder and a carry-look-ahead (CLA) circuit for 8 bit adder.

We confirmed the circuit operation by using computer simulation. Each of add time in the 8 bit RC and CLA adders was evaluated (all of MOSFET were set to W/L＝1 μm/0.35 μm except for M24 (W/L＝1.5 μm/0.35 μm)). The add time was derived from the longest calculation of 11111111 + 00000001 = 100000000. Figure 10 shows the waveforms of each bit output voltage. The time was calculated by the delay time of highest-order bit of output S7. The monitor current I_0 in the power supply circuit was set to 10 nA. The add time of RC adder was 5.1 μs (Fig. 10(a)), and that of CLA adder was 3.4 μs (Fig. 10(b)). The number of threshold logic gates from lowest-order bit input (X0 Y0) to highest-order output bit S7 is nine in a ripple carry adder, and five in a carry-look-ahead adder.

6. Conclusion

We proposed threshold logic systems consisting of subthreshold MOSFETs circuits. The circuit can be constructed with simple circuit configuration and low power dissipation, and can be used for an elementary cell for large-scale parallel signal processing, such as image-processing and neural network applications. As an example subsystem, we also developed 8 bit adders by using majority decision gates. As a future work, we will develop and fabricate a functional signal processing by using a threshold logic gate.

Reference

[1] Saburo Muroga, *Threshold logic and its applications*, Wiley Interscience, 1971.

[2] A. Wang, B.H. Calhoun, A.P. Chandrakasan, *Sub-threshold Design for Ultra Low-Power Systems*, Springer, 2006.

[3] Hirose T., Asai T., and Amemiya Y., "Power-supply circuits for ultralow-power subthreshold MOS-LSIs," *IEICE Electronics Express*, vol. 3, no. 22, pp. 464-468 (2006).

[4] Hirose T., Matsuoka T., Taniguchi K., Asai T., and Amemiya Y., "Ultralow-power current reference circuit with low temperature dependence," *IEICE Transactions on Electronics* vol. E88-C, no. 6, pp. 1142-1147 (2005).