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Single-Electron Logic Systems Based on the Binary Decision Diagram

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SUMMARY This paper proposes a method of constructing single-electron logic subsystems on the basis of the binary decision diagram (BDD). Sample subsystems, an adder and a comparator, are designed by combining single-electron BDD devices. It is demonstrated by computer simulation that the designed subsystems successfully produce, through pipelined processing, an output data flow in response to the input data flow. The operation error caused by thermal agitation is estimated. An output interface for converting single-electron transport into binary-voltage signals is also designed.

key words: *binary decision diagram, BDD, single electron, logic circuit, adder, comparator*

1. Introduction

One of the present challenges in microelectronics is to develop ultrahigh-density and low-power LSIs based on single-carrier electronics. To create such LSIs, we must employ a new paradigm for digital processing that makes the best use of single-electron transport. This paper proposes a promising approach, a method of *constructing single-electron logic systems on the basis of the binary decision diagram.*

In single-carrier electron technology, electronic functions are manipulated by controlling the transport of individual electrons, using a single-electron circuit. Because the single-electron circuit is quite different in its principle of operation from ordinary transistor circuits, we must develop a new circuit architecture in which large logic systems can be constructed easily by utilizing the properties of single-electron transport. Two years ago, the authors suggested that the binary decision diagram (BDD), a graphical method for representing digital functions, can be utilized for constructing large single-electron logic circuits [1]. In a subsequent paper [2], we proposed the guiding principle for constructing single-electron logic circuits on the basis of BDD architecture. We designed several elemental logic circuits such as NAND, NOR, and XOR logic gates, and then showed by computer simulation that the designed circuits produced correct logic operations.

In this paper, we will show that single-electron BDD logic circuits of greater complexity can be constructed easily by following the guiding principle that we have proposed. In the following sections, we will first outline the single-electron BDD device, which we proposed in our earlier paper (Sect. 2). After that, we will construct sample logic subsystems by using the BDD devices. We will design an adder and a comparator by combining the devices, and then will simulate the operation of the design subcircuits to demonstrate that correct logic operations can be obtained (Sect. 3). The operation error caused by thermal agitation will also be estimated (Sect. 4). Finally, we will present the construction of an output interface circuit for converting single-electron transport into binary-voltage signals (Sect. 5).

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2. The Single-Electron BDD Device

2.1 The Concept of the BDD

The binary decision diagram is a way of representing digital functions by using a directed graph, rather than a Boolean expression. (See Refs. 3 and 4 for details.) A BDD is a graph composed of many nodes and two terminals, with each node labeled by a variable. Several examples of the BDD are illustrated in Fig. 1. In determining the value of the function for a given set of variables, we enter at the root and proceed downward to a terminal. At each node, we follow the branch corresponding to the value of the variable X_i; that is, we follow the 1 branch if $X_i = 1$ and the 0 branch if $X_i = 0$. The value of the function is equal to the value of the terminal we reach; the function is 1 if we reach the 1-terminal, and 0 for the 0-terminal. The BDD was conceived and developed as a convenient tool for computer-aided logic design and provides concise expression for most digital functions encountered in logic design applications.

2.2 Single-Electron BDD Device

In our earlier paper [2], we presented the idea of materializing the BDD by using a single-electron circuit. A BDD consists of many nodes, and the function of each node is two-way switching controlled by an input variable. To implement this function, we proposed using a differential single-electron switch, illustrated in

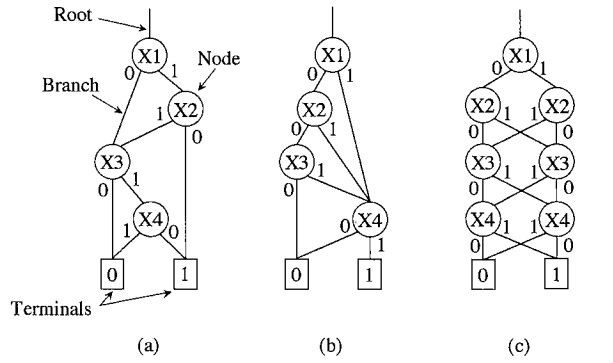

Fig. 1 Examples of BDD: construction for logic of (a) $X1\overline{X2}+X3\overline{X4}$, (b) $(X1+X2+X3)X4$, and (c) odd parity.

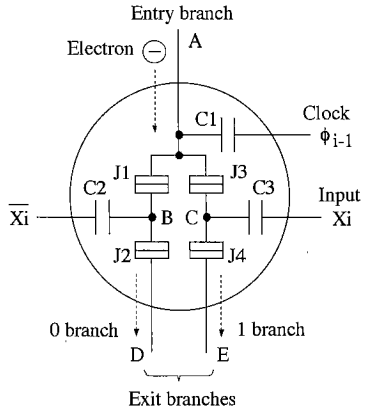

Fig. 2 The BDD device consisting of a single-electron circuit. Its function is two-way switching for electron transport.

Fig. 2, which we named *the BDD device* (for details, see Ref. 2). The device consists of four tunnel junctions (J_1 through J_4) and three capacitors (C_1 through C_3), with an entry branch (A) and two exit branches (D and E), and is driven by a voltage clock (ϕ_{i-1}). A binary voltage input X_i (and its complement $\overline{X_i}$), specifying the value of a variable, is applied to island C (and B) through capacitor C_3 (and C_2). The device operates as a two-way switch that accepts an electron from the entry branch and sends the electron to either exit branch; it transfers an electron along the path of $A \rightarrow C \rightarrow E$ if X_i is an appropriate positive voltage, and transports as $A \rightarrow B \rightarrow D$ if X_i is a negative.

2.3 Construction of BDD Logic Systems

A logic circuit is constructed by connecting many identical BDD devices into a cascade to build the tree of a BDD graph. The entire system is composed of the BDD tree circuit, an electron injector, and an output circuit, as illustrated in Fig. 3. At start of operation, a single electron (called a *messenger electron*) is injected from the electron injector into the root node and then transferred by four clocks (ϕ_0 through ϕ_3) through the

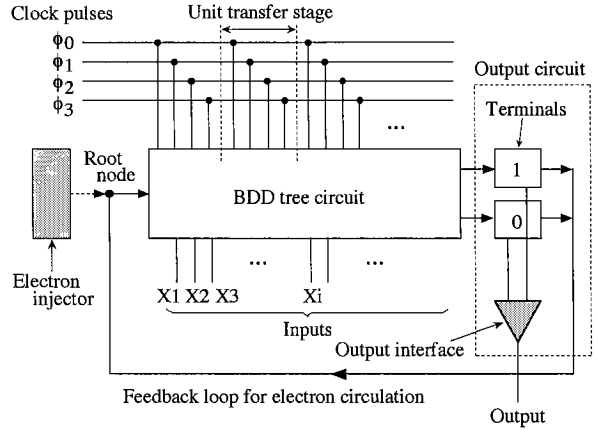

Fig. 3 Schematic view of the entire system, consisting of a BDD circuit (a tree circuit and terminals), an electron injector, and an output circuit.

BDD tree circuit to a terminal. The messenger electron travels along the BDD path specified by a given set of inputs $(X_1, X_2, \ldots)$. The value of the logic is determined by observing which terminal the messenger electron reaches. To produce a voltage output corresponding to the logic value, an output interface is used. The messenger electron ejected from a terminal is returned to the root node through the feedback loop to be used for successive logic operation.

3. Construction of Subsystems Using Single-Electron BDD Devices

Any combinational logic can be implemented by combining identical BDD devices. We here present sample designs of two subsystems, specifically, circuits for an adder and a comparator, and show their operation by computer simulation. For each subsystem, we will give first the configuration of the corresponding BDD, and then will produce a single-electron circuit that implements the given BDD. In calculating the circuit operation, we used the Monte Carlo method combined with the basic equations for electric-charge distribution, charging energy, and tunneling probability (for this method, see Ref. 5. Also see Appendix.).

3.1 Adder

We will take up as an example a 4-bit adder. It accepts two 4-bit adder inputs (an addend and an augend) and produces the corresponding 4-bit sum output and 1-bit carry output. We hereafter represent the two adder inputs by binary numbers $a_3a_2a_1a_0$ and $b_3b_2b_1b_0$, the adder output by $s_3s_2s_1s_0$, and the carry output by c_3, where the value of each element a_3 through c_3 is either 1 or 0.

The operation of the adder is represented by using a set of BDD graphs as illustrated in Fig. 4. Each bit of the outputs (s_0 through s_3 and c_3) is produced

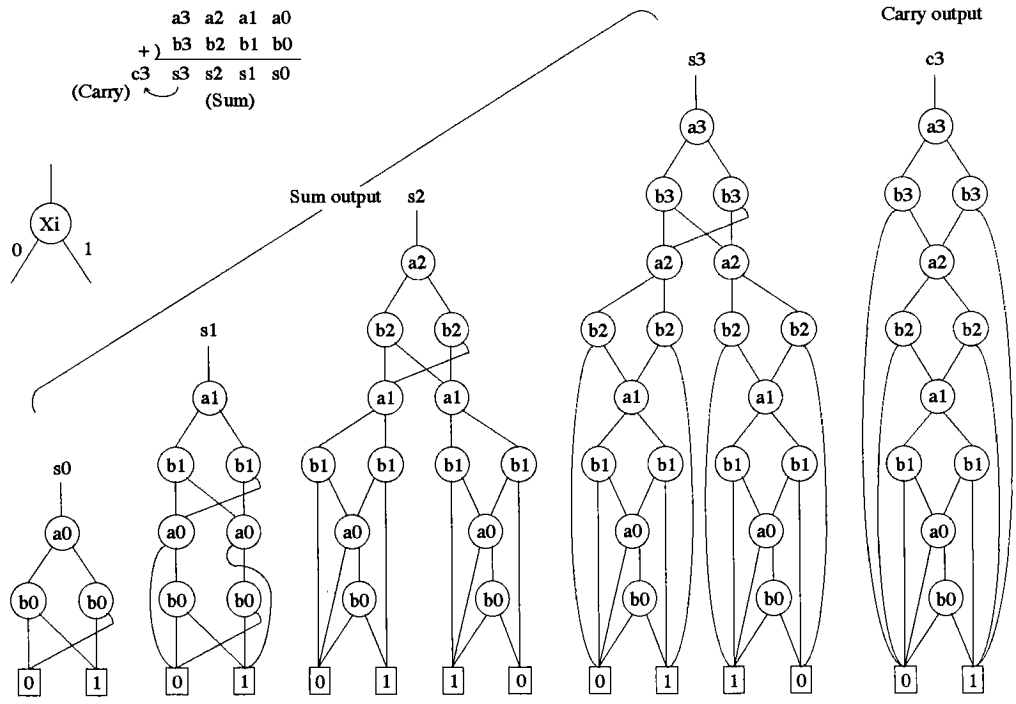

Fig. 4 A set of BDD graphs for a 4-bit adder: s_0 through s_3 denote the sum output sum bits, and c_3 denotes the carry output bit.

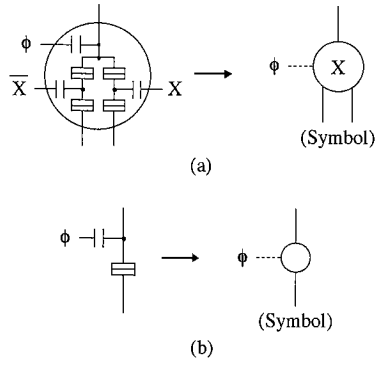

Fig. 5 Symbols for illustrating the designed circuits: the symbol for (a) the BDD device and (b) the buffer.

by the corresponding BDD graph, which contains the value of the input bits (a_0 through a_3 and b_0 through b_3) as node variables. In this illustration, we define that, in each node, the exit branch on the right side shows a 1 branch and the exit branch on the left shows a 0 branch.

We designed the single-electron circuits that implement the BDDs above. Before presenting the designed circuits, we will give in Fig. 5 two symbols for illustrating the designed circuits. One is a symbol for the BDD device (Fig. 5 (a)) and the other is for a buffer (Fig. 5 (b)). The buffer is a subcircuit consisting of a tunnel junction and a capacitor. Its function is to set up a *dummy node* and hold a messenger electron for one clock period - an indispensable element for constructing a single-electron BDD circuit.

The circuits designed for the adder are illustrated in Fig. 6. In each circuit, a root node is indicated by the boxed word *Root*, and terminal nodes are indicated by the boxed numerals **1** and **0**. The configuration of each circuit was obtained by replacing the nodes in the BDDs of Fig. 4 with BDD devices. Factors to keep in mind in designing the circuit include the following.

1. To transfer and circulate the messenger electron in the circuit, the four-phase (ϕ_0 through ϕ_3) clock is applied to BDD devices and buffers. (The phase shift of the clock is: $\phi_0 = 0$, $\phi_1 = -\pi/2$, $\phi_2 = -\pi$, $\phi_3 = -3\pi/2$.) The bit signals of the adder inputs are applied in sequence to the BDD devices such that the bit signal for a BDD device is applied synchronously with the clock pulse for the consecutive BDD device (or the consecutive buffer).

2. In actual systems, an input-bit signal will be applied to all the BDD circuits simultaneously with the clock. For successful circuit operation in such a situation, buffers (dummy nodes) are set up on appropriate points on the path to ensure that a messenger electron will arrive at each BDD device at the correct time.

3. Two or more messenger electrons can be used in a BDD circuit. Putting a messenger electron on every transfer stage (a subcircuit that is driven by a set

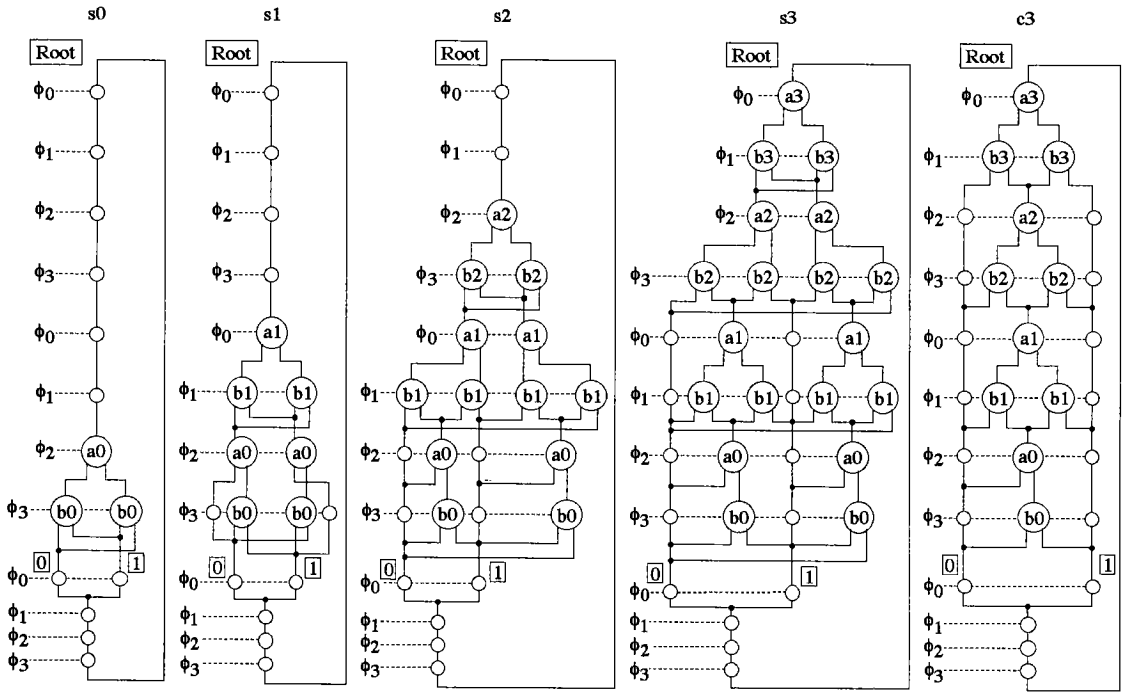

Fig. 6 Single-electron BDD circuits for a 4-bit adder. The configuration of each circuit was obtained by replacing the nodes in the BDDs of Fig. 4 with BDD devices.

of four clock pulses) produces a pipelined operation that improves the processing throughput. In the present instance, three messenger electrons can be put in each BDD circuit.

We simulated the add operation of the designed adder system and confirmed correct operation for all combinations of inputs (256 patterns). The parameters used were: junction capacitance = 10 aF and tunnel resistance = 100 kΩ for each tunnel junction, capacitance = 10 aF for each capacitor, and temperature = 0 K. Three messenger electrons were put in each BDD circuit. A portion of the simulation result is illustrated in Fig. 7. Plotted are the waveforms for clock pulse ϕ_0 (the other clocks are omitted), input-bit pulses (a_3 through b_0), and output charges (s_0 through c_3, the charges on the 1-terminal nodes of the four BDD circuits, normalized to the electron charge). The adder system produced an output data flow in response to the input data flow, as a linear systolic array; in the figure, a set of input and output data is marked by a gray line. One logic operation (from accepting a_3 to producing the corresponding output) requires 8 ns, but owing to the pipelined processing we can obtain output data every 4 ns.

3.2 Comparator

The function of a comparator is to compare two given variables to determine which variable is larger (or smaller). We here take up a 4-bit comparator as an example. It accepts two 4-bit inputs (A and B, $A = a_3a_2a_1a_0$ and $B = b_3b_2b_1b_0$) and produces three 1-bit outputs (s_1, s_2, and s_3). The required outputs are: $s_1 = 1$ and $s_2 = s_3 = 0$ if $A > B$, $s_2 = 1$ and $s_1 = s_3 = 0$ if $A = B$, and $s_3 = 1$ and $s_1 = s_2 = 0$ if $A < B$.

The operation of the comparator is represented by using a set of BDD graphs as illustrated in Fig. 8. Each of the output bits (s_1, s_2, s_3) is produced by the corresponding BDD graph. (In each node, the exit branch on the right side shows a 1 branch and the exit branch on the left shows a 0 branch.)

We designed the single-electron circuits that implement the BDDs above. The result is illustrated in Fig. 9. To operate the circuits successfully under clocked operation, the buffers were set up on appropriate points on the path of a messenger electron.

The operation of the designed comparator was simulated for all the input combinations, to confirm correct operation. (The same parameters as for the adder were used. Three messenger electrons were put in each BDD circuit.) A portion of the simulation result is illustrated in Fig. 10. Plotted are the waveforms for clock pulse ϕ_0, input-bit pulses (a_3 through b_0), and output charges (s_1 through s_3, the charges on the 1-terminal nodes of the three BDD circuits, normalized to the electron charge). The comparator system produced output data every 4 ns as a result of pipelined processing.

4. Operation Error Caused by Thermal Noise

In operating a single-electron circuit, the important is-

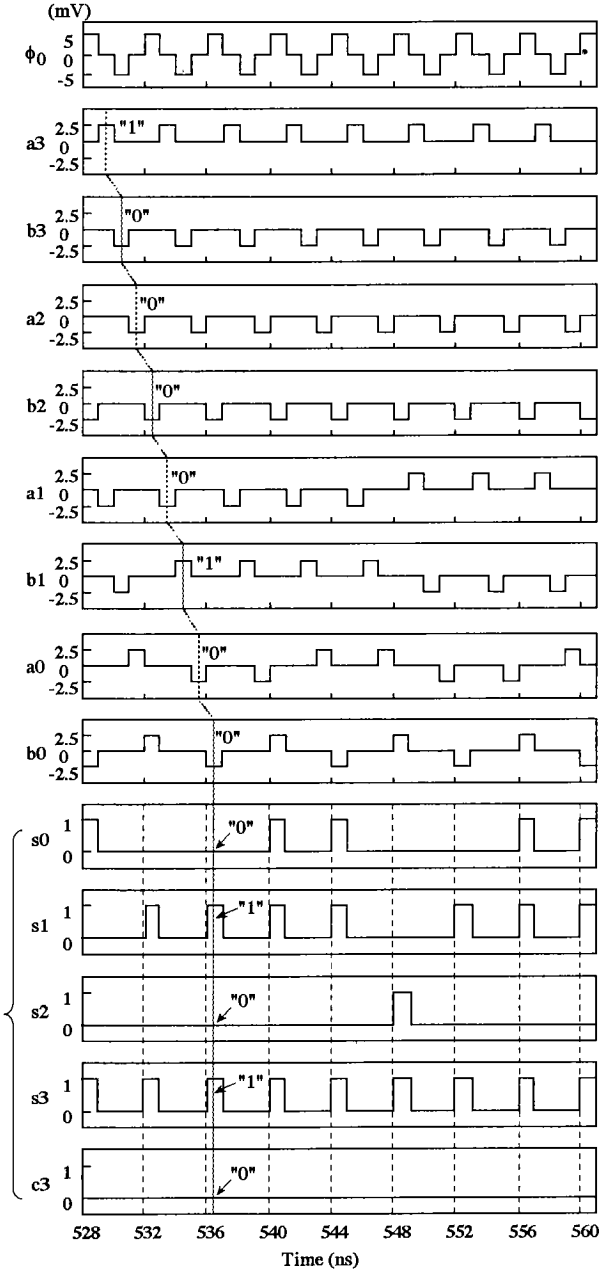

Fig. 7 A portion of the simulation result for the operation of the adder circuits in Fig. 6. Plotted are the waveforms for clock pulse ϕ_0, input-bit pulses (a_3 through b_0), and output charges (s_0 through c_3, the charges on the 1-terminal nodes of the four BDD circuits, normalized to the electron charge). For device parameters, see the text.

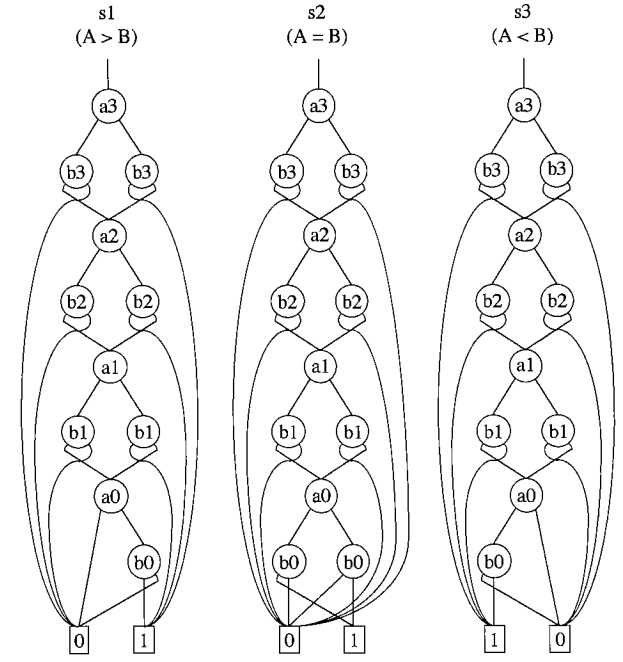

Fig. 8 A set of BDD graphs for a 4-bit comparator: s_0 through s_3 denote the output bits.

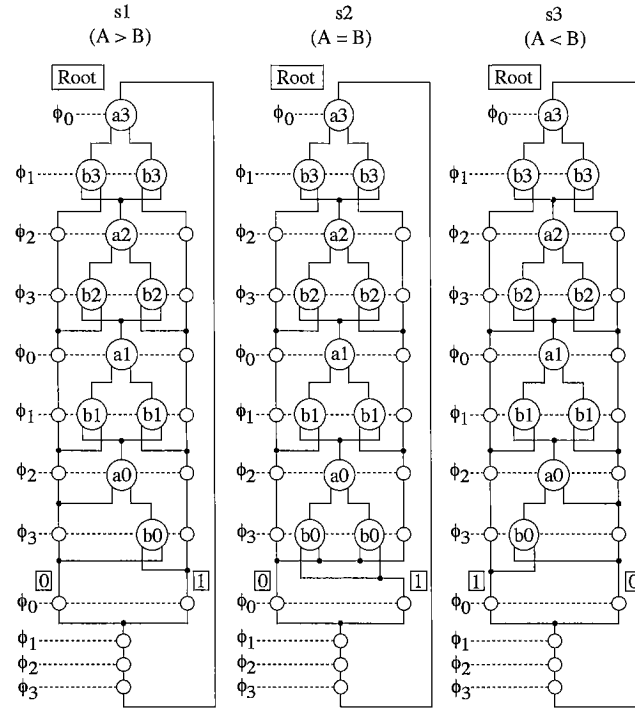

Fig. 9 Single-electron BDD circuits for a 4-bit comparator.

sue to be addressed is operation error caused by an unexpected tunneling induced by thermal agitation. ("Unexpected tunneling" means a tunneling that does not follow the BDD path.) The error rate for a given BDD circuit can be estimated from the mean tunneling rate for each tunneling event in the circuit (see Ref. 2 for the error-estimation procedure). We calculated the error rate for the adder system discussed in Sect. 3.1, and illustrate the result in Fig. 11.

There are two ways to reduce the operation error. One is to scale down the capacitance parameters in the circuits. The limit of the operation temperature will increase in proportion to the scaling-down rate for the

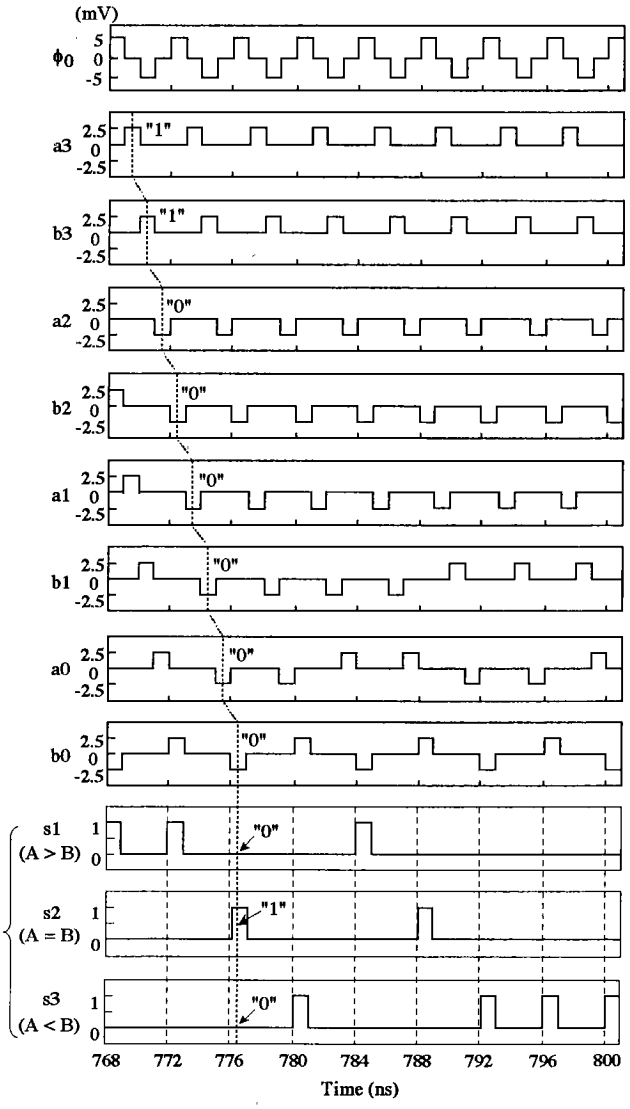

Fig. 10 A portion of the simulation result for the operation of the comparator circuit in Fig. 9. Plotted are the waveforms for clock pulse ϕ_0, input-bit pulses (a_3 through b_0), and output charges (s_0 through s_3, the charges on the 1-terminal nodes of the three BDD circuits, normalized to the electron charge).

capacitance parameters. The other way is to employ the method of majority decision, in which the output is decided by the majority of logic operation trials. For details, see Ref. 2.

5. Circuit for the Output Interface

As described in Sect. 3, the value of the logic in a single-electron BDD circuit is determined by observing which terminal node a messenger electron passes through. For practical applications, it is desirable that the output be obtained in the form of a voltage signal; that is, a BDD circuit should be constructed such that it produces a high voltage if a messenger electron passes through a 1-terminal node, and a low voltage if it passes through a 0-terminal node.

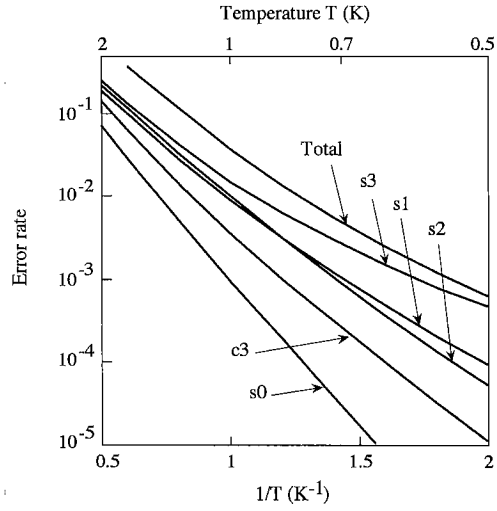

Fig. 11 Calculation results for the rate of thermal error in the 4-bit adder circuit of Fig. 6.

For this purpose, we designed an output interface circuit. It is a single-electron latch, illustrated in Fig. 12. This circuit accepts a differential input (*input* and $\overline{input}$) and produces a differential output (*output* and $\overline{output}$). *Input* is connected to a 1-terminal node in a BDD circuit, and $\overline{input}$ to a 0-terminal node. If a messenger electron in the BDD circuit reaches the 1-terminal node, the potential of input turns low, then the latch circuit will produce a high voltage on *output* and a low voltage on $\overline{output}$ (output "1"). And if a messenger electron reaches the 0-terminal node, the potential of *output* will turn low and $\overline{output}$ will turn high (output "0"). A sample set of capacitance parameters for successful operation is illustrated in the figure. Under this parameter set, the latch circuit had a stability diagram as illustrated in Fig. 13, where a set of numbers, e.g., (0,0,−1,0), indicates the numbers of excess electrons stored on islands P, Q, R, and S in the circuit. The state (0,0,−1,0) produces an output "1" (*high-output region*) and the state (−1,0,0,0) produces an output "0" (*low-output region*).

We operated the latch circuit under conditions such that the operating point moved on around the A, B, and C in Fig. 13. In the region around point B, two states (0,0,−1,0) and (−1,0,0,0) overlapped, so the latch circuit had two stable states in this region and maintained its state the same as it was just before entering this region. This bistability is very useful for interface operation, as described in the following.

We simulated operation of the designed latch circuit. The result is illustrated in Fig. 14. The latch was connected to terminal nodes of a BDD circuit, and its output was observed. Plotted in the figure are the waveforms for the normalized charges on the 1-terminal and the 0-terminal ((a), (b)), the potential on the terminals

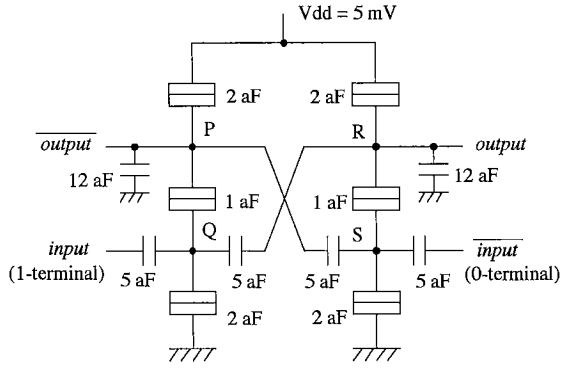

Fig. 12 Single-electron latch for an output interface.

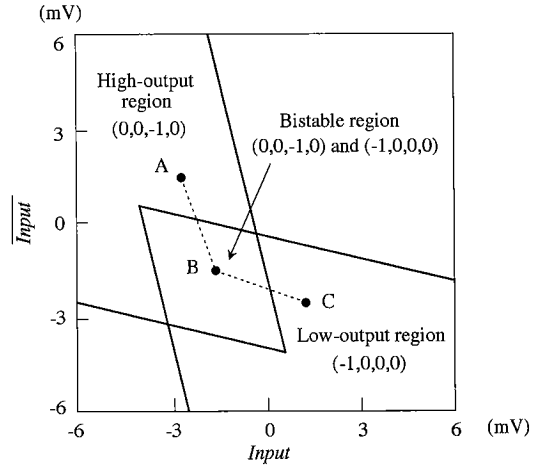

Fig. 13 Stability diagram for the latch circuit in Fig. 12.

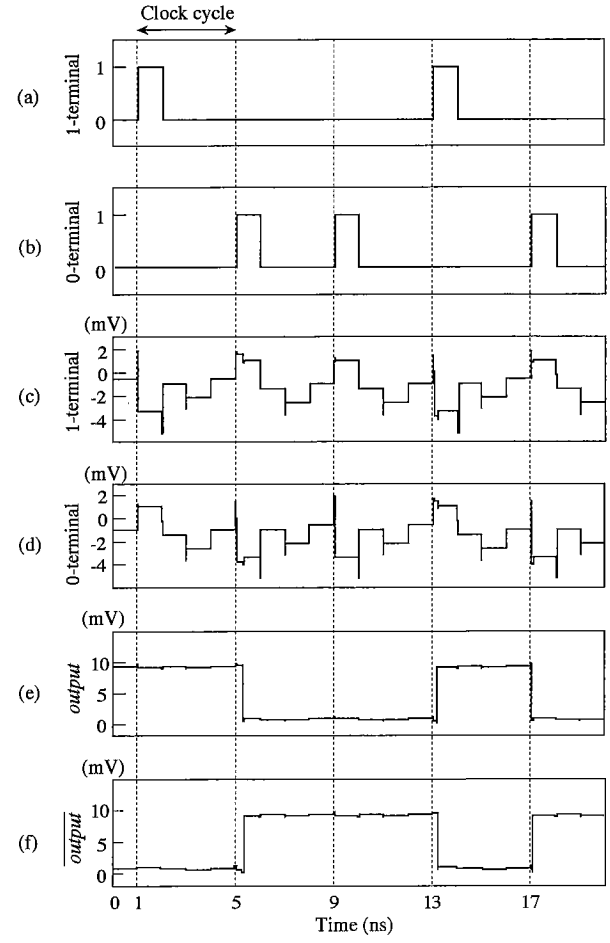

Fig. 14 Simulation result for the operation of the latch circuit connected to terminal nodes of a BDD circuit. Plotted are the waveforms for the normalized charges on the 1-terminal and the 0-terminal ((a) and (b)), the potential on the terminals ((c) and (d)), and the output voltages (*output* and $\overline{output}$) of the latch ((e) and (f)).

((c), (d)), and the output voltages (*output* and $\overline{output}$) of the latch circuit ((e), (f)). The potential waveforms for the terminals included noise induced by clock pulses, as shown in the figs. (c) and (d). To obtain the logic output correctly under such conditions, we determined the capacitance parameters for the latch circuit so that the operating point would move around within the *bistable region* when no messenger electron existed on the terminal nodes, and the operating point would move to the *high-output* (*low-output*) *region* when a messenger electron arrived at the 1-terminal (0-terminal) node. (An optimum parameter set is given in Fig. 12.) In this way we could obtain the logic output correctly, as illustrated in Figs. 14 (e) and 14 (f); the noise disappeared in the output waveforms and the output value was held for one clock cycle.

6. Conclusion

This paper proposed a method of constructing single-electron logic systems on the basis of the binary decision diagram. Following the guiding principle that we have proposed, we designed sample logic subsystems, an adder and a comparator, by combining single-electron BDD devices. Matters that require attention in designing the subsystems were discussed. The operation of the designed subsystems was calculated by computer simulation. It was demonstrated that the designed subsystems successfully produce an output data flow in response to the input data flow through pipelined processing. The operation error caused by thermal agitation was estimated. An output interface for converting single-electron transport into binary-voltage signals was also designed.

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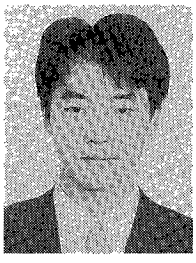
Appendix

The authors will offer gratis the programs of the single-electron circuit simulator used in this paper. This simulator is based on the Monte Carlo method and can analize operation of single-electron circuits consisting of tunnel junctions (tunnel-junction capacitors), ordinary or nontunnel capacitors, and voltage sources for power, clocks, and signal inputs. The simulator accepts as input a circuit netlist described in a similar form to that for ordinary circuit simulators such as SPICE. If you want to try this simulator, please do not hesitate to contact us. The electronic-mail address is: asahi@sapiens.huee.hokudai.ac.jp.



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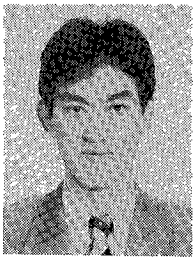

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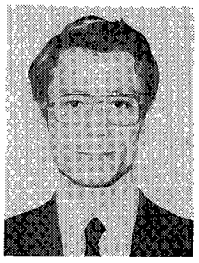

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