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Multiple-Valued Inverter Using a Single-Electron-Tunneling Circuit

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SUMMARY A multiple-valued logic inverter is proposed that uses single-electron-tunneling (SET) circuits in which the discreteness of the electron charge is utilized. The inverter circuit, which is composed of only two SET transistors, has a memory function as well as an inverter function for multiple-valued logic. A quantizing circuit and a D flip-flop circuit for multiple-valued logic can be compactly constructed by combining two inverters. A threshold device can be compactly constructed by attaching more than one input capacitor to the inverter circuit. A quaternary full adder circuit can be constructed by using two threshold devices. Implementation issues are also discussed.

key words: *single electron, SET, multiple-valued, Coulomb blockade*

1. Introduction

A promising area of research in microelectronics is the development of integrated circuits based on single-carrier electronics. In this paper, we propose a multiple-valued inverter circuit constructed of single-electron-tunneling (SET) circuits.

Single-carrier electronics is a technology for manipulating electronic functions by controlling the transport of indivisual electrons, utilizing the SET phenomenon [1]. This technology has been receiving increasing attention because it affords the possibility of producing LSI circuits that have both dense integration and low power dissipation. It is natural for us to hit upon the idea of using the discrete charge of an individual electron for generating multiple-valued signals in SET circuits. Using multiple-valued logic (MVL) in an electronic circuit would lead not only to an increase in the density of integration but also to an increase in processing speed and a reduction in the number of the interconnections [2]. MVL circuits could also be used to construct fuzzy, fault-tolerant, asynchronous systems [2]–[4]. Toward this goal, we must find ways to generate, store, and transfer multiple-valued signals in SET circuits.

The inverter is one of the basic logic gates, and it can be used to construct a threshold device that is useful for building a multiple-valued logic system. We propose a multiple-valued inverter that uses SET circuits and describe its design methodology, its function and its reliability. The next section describes the design method of proposed inverter circuit. A way to construct a quantizing circuit is also shown. Section 3 describes the circuit's inverter function for multiple-valued logic and its memory function. It is shown that a multiple-valued D flip-flop circuit, which is normally a large circuit, can be compactly constructed. Section 4 describes a way to construct a multiple-valued threshold device. Section 5 discusses implementation issues. Section 6 is a brief summary.

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2. Multiple-Valued Inverter Circuit

A SET multiple-valued inverter circuit can be obtained by adjusting the parameters of the quasi-CMOS inverter circuit proposed by Tucker [5]. In this section, we describe the quasi-CMOS inverter circuit, and the design method of the multiple-valued inverter circuit.

2.1 Quasi-CMOS Inverter Circuit

The SET circuit shown in Fig. 1(a) is called a "quasi-MOSFET." It consists of two tunneling junctions and two capacitors. By controlling the bias voltage applied to the back gate, we can adjust its Coulomb blockade condition. The behavior of this device is similar to that of an nMOSFET or a pMOSFET when a high or a low voltage is applied to the back gate. A quasi-CMOS inverter circuit [5] that operates like a CMOS inverter can be constructed by connecting two quasi-MOSFETs through the load capacitance C_L as shown in Fig. 1(b). The capacitances were initially chosen as follows [5];

$$\begin{aligned} &C_{j1} = 1\,\mathrm{aF},\ C_{j2} = 2\,\mathrm{aF},\ C_G = 8\,\mathrm{aF}, \\ &C_B = 7\,\mathrm{aF},\ C_L = 24\,\mathrm{aF}. \end{aligned} \tag{1}$$

In Fig. 1(b), L, M, and N represent the islands between the tunneling junctions. When there is an excess hole at M, the device outputs a high voltage. When there is no excess charge at M, it outputs a low voltage. The quasi-MOSFET above the output node (the *quasi-pMOSFET*) and the quasi-MOSFET below the output node (the *quasi-nMOSFET*) operate in a complementary manner as follows.

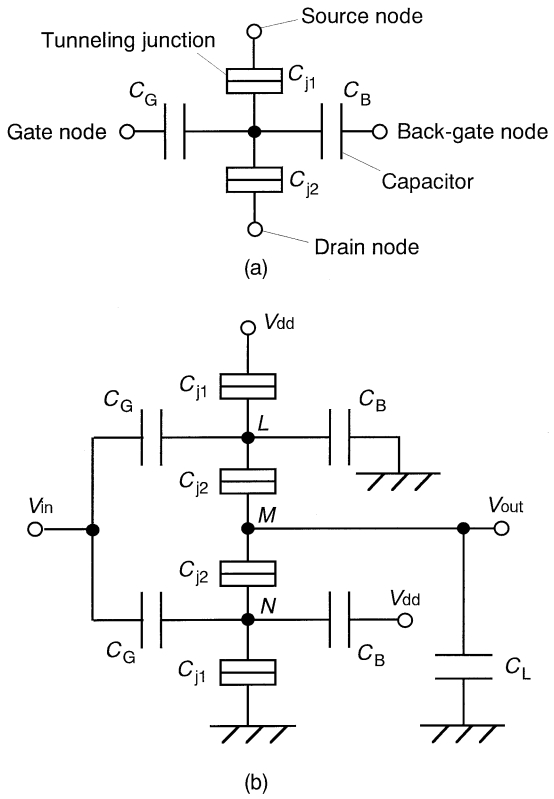


Fig. 1 Circuit diagrams for (a) a quasi-MOSFET, and (b) a quasi-CMOS inverter circuit that can be made into a multiple-valued inverter by adjusting the parameters.

1) When the input voltage is low, the quasi-nMOSFET stabilizes because of the Coulomb blockade for both high and low output signals. The quasi-pMOSFET becomes unstable (the Coulomb blockade is destroyed) if the output voltage is low, and it becomes stable (the Coulomb blockade is achieved) if the output voltage is high. If the output voltage is low, i.e., M has no excess charge, an electron is transferred from M to voltage source V_{dd} through the quasi-pMOSFET. This leaves a hole at M that causes the output voltage to become high, which stabilizes the quasi-pMOSFET. As a result, the entire circuit becomes stable and outputs a high voltage.

2) When the input voltage is high, the quasi-pMOSFET stabilizes for both high and low output signals. The quasi-nMOSFET becomes unstable if the output voltage is high, and it becomes stable if the output voltage is low. If the output voltage is high, i.e., M has one hole, an electron is transferred from the ground to M through the quasi-nMOSFET, and the charge vanishes at island M. This causes the output voltage to become low, which stabilizes the quasi-nMOSFET. As a result, the entire circuit becomes stable and outputs a low voltage.

2.2 Parameters for a Multiple-Valued Inverter Circuit

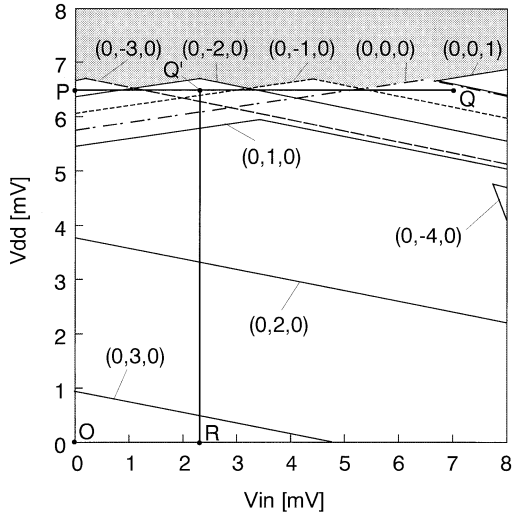
Using the circuit shown in Fig. 1(b), a multiple-valued signal can be generated by adjusting the magnitude of the capacitances C_G, C_B, and C_L, and fixing the values of C_{j1} and C_{j2}. A quaternary device can be designed as follows. The value of C_L should be 72 aF to store three holes and to make the maximum output voltage around 6.5 mV. Then the values of C_G and C_B should be adjusted so that the proper multiple-value is output. A useful tool for this adjustment is a stability diagram that shows Coulomb blockade condition on the bias voltage plane. By plotting the stability diagram repeatedly after slightly changing the values of C_G and C_B, we found the following parameters;

$$C_{j1} = 1\,\text{aF},\ C_{j2} = 2\,\text{aF},\ C_G = 2\,\text{aF},\\ C_B = 10\,\text{aF},\ C_L = 72\,\text{aF}. \tag{2}$$

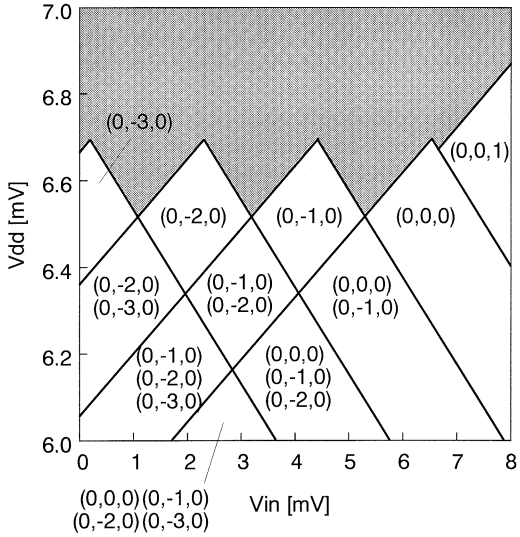
The stability diagrams for parameter set (2) are shown in Fig. 2. They are plotted on the V_{in}-V_{dd} plane and show the Coulomb blockade bias condition for several internal states. The white regions are the stable regions where the Coulomb blockade occurs. The shaded region is an unstable region where tunnelings frequently occur. In Fig. 2(a), various stable regions overlap in a complex manner. Figure 2(b) is an enlargement that more clearly shows the relation among the stable regions. In both figures, the internal state of the circuit is given by (l, m, n), where l, m, and n are the number of electrons that can exist at islands L, M, and N, respectively. Except for $(0, -4, 0)$ and $(0, 0, 1)$, all regions are located so as to contain the origin. m mainly determines the output voltage, while l and n slightly modify the output voltage. Increasing m, which can take a negative value to represent the number of holes, decreases the output voltage. $(0, -3, 0)$, $(0, -2, 0)$, $(0, -1, 0)$ and $(0, 0, 0)$ are used to output multiple values "3," "2," "1," and "0," respectively.

A multiple-valued inverter operation can be achieved by moving the bias point along the PQ locus in Fig. 2(a). Because the bias point moves across four stable regions with different m's, the transfer characteristic should look like a staircase. This transfer characteristic was simulated by a Monte Carlo method that took into account the basic equations for electric-charge distribution, charging energy, and tunneling probability ignoring the cotunneling [6]. The result is shown in Fig. 3. Here the temperature is assumed to be 0 K. Though hysteresis exists in the transfer characteristic, it is not a problem for discrete input voltages that are all located outside the hysterisis loop. The Monte Carlo simulation showed that a cascade connection of more than two inverter gates achieves a successful signal transfer.

By cascading two inverter circuits, we can obtain a quantizing circuit as shown in Fig. 4. A multiple-valued



(a)



(b)

Fig. 2 Stability diagram for parameter set (2). The shaded region is an unstable region. The boundary of each region is denoted by the stable electron state of its region. (b) enlarged stability diagram.

quantizing circuit can be used as an analogue-digital converter and as a buffer for adjusting the multiple value. In a quantizing circuit, the multiple-valued output increases monotonously with the input voltage. In Fig. 4, a quantizing function is obtained by connecting voltage source V_{dd} to nodes V_A and V_B. The simulated transfer characteristic of this circuit for $V_{dd} = 6.5\,\mathrm{mV}$ at 0 K is shown in Fig. 5. By using SET circuits, a quantizing circuit with a simple configuration can be obtained.

3. Memory Function

It may be possible to get the potential functions of an

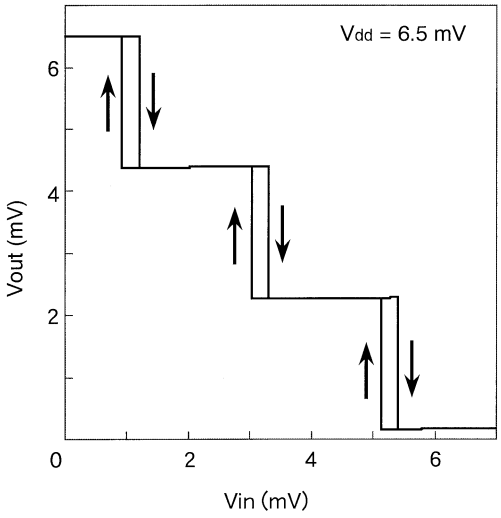


Fig. 3 Transfer characteristic of multiple-valued inverter circuit.

SET device from the stability diagram [7]. As shown in Fig. 2(a), more than two stable regions overlap at the origin, which makes the circuit multi-stable at the bias point O. This characteristic can be exploited to create an inverted multiple-valued memory function. If we move the bias point along the locus P→Q′ →R→O, the electron arrangement becomes $(0, -2, 0)$ at Q′, and it can be maintained at point O. Therefore, the stored information can be maintained after V_{dd} and V_{in} are turned off. We carried out a Monte Carlo simulation of this function. As shown in Figs. 6(a) through (c), the inverted values of the input multiple-values can be retained after turning off the voltage bias. The duration of the clock is determined as follows. To prevent stochastic errors due to tunneling, the duration of the clock pulse should be long enough to complete the transition. Among the possible transitions of the internal state, the one having the longest mean waiting time of one inverter is $(0, -3, 0) \rightarrow (0, -3, 1) \rightarrow (0, -2, 0) \rightarrow (0, -2, 1) \rightarrow (0, -1, 0) \rightarrow (0, -1, 1) \rightarrow (0, 0, 0)$. When the tunneling resistance R_T of each tunneling junction is 1 MΩ, the tunneling rate Γ of this transition at 0 K is 3.8×10^8/s. To keep the error rate below 10^{-9} at 0 K, the duration τ of the clock pulse should satisfy the following relation, which is based on the theory described in Ref. [8].

$$\tau\Gamma > 20 \tag{3}$$

The duration should thus be longer than 53 ns. In Fig. 7, the duration of the clock pulse is 60 ns.

In the same way, by applying a clock pulse at V_A and V_B, the circuit in Fig. 4 can store a multiple-valued input. This function was also simulated, and the result is shown in Fig. 6(d).

Next we describe how to construct a sequential circuit (a D flip-flop). A D flip-flop circuit stores the input

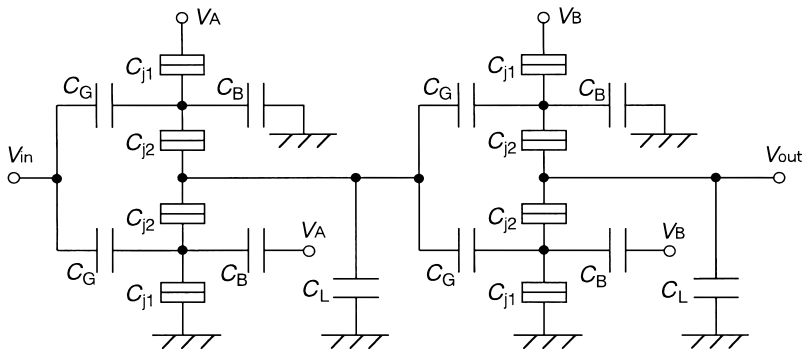


Fig. 4 The cascade connection of two inverters. This circuit can be used as a quantizing circuit, as a memory, or as a D flip-flop.

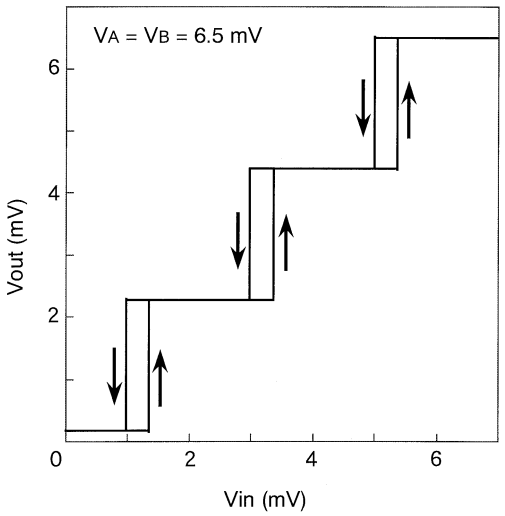


Fig. 5 Transfer characteristic of the quantizing circuit shown in Fig. 4 for $V_A = V_B = 6.5\,\mathrm{mV}$.

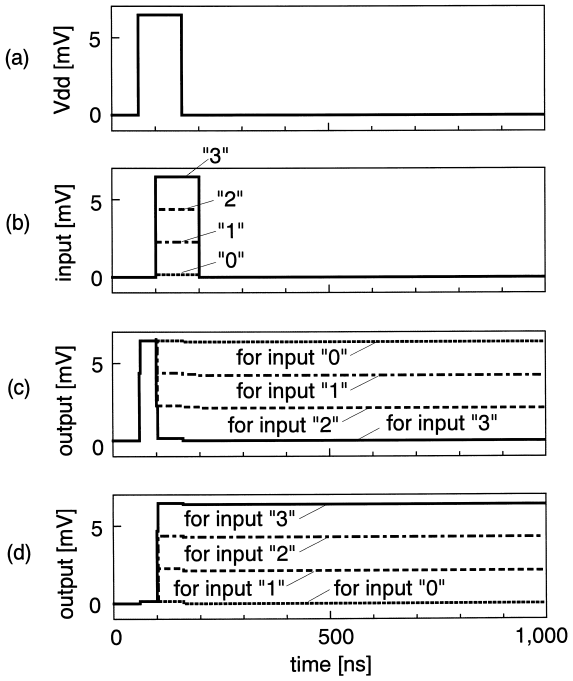


Fig. 6 Simulated waveforms of the memory function. (a) V_{dd}, (b) input value, (c) the output of multiple-valued inverter shown in Fig. 1 and (d) the output of quantizing circuit shown in Fig. 4.

value at the edge of the clock pulse. In the stability diagram (Fig. 2(a)), the circuit is multi-stable on the input-voltage axis. Therefore, we can create a latch function that maintains the output signal and ignores any input signal. A D flip-flop circuit can thus be obtained by using the circuit construction shown in Fig. 4 if the clock signal CLK is applied to node V_B, and the inverted clock signal $\overline{CLK}$ is applied to node V_A. For $CLK = 0$, the first inverter changes its state depending on the value of V_{in}, but the second one does not. For $CLK = 1$, the first inverter's state is independent of the input signal, while the second one sets and maintains its output based on the signal received from the first one. We again used a Monte Carlo simulation to generate the waveforms of this function. As shown in Fig. 7, the input signal is stored when the clock voltage is high, and the stored value is maintained after the clock signal is turned off.

4. A Way to Construct a Multiple-Valued Logic Circuit

As described above, one way to construct a multiple-valued circuit is to use a multiple-valued threshold device. A schematic diagram of the quaternary threshold device and its characteristic is shown in Fig. 8. The threshold device receives more than one input signal, weights each input, sums up all the weighted-inputs, compares the sum with the threshold values t_i, and then outputs a multiple-valued signal V_{out}. The value of V_{out} depends on the value of the sum of weighted input. For an example, a quaternary threshold device changes its output as follows;

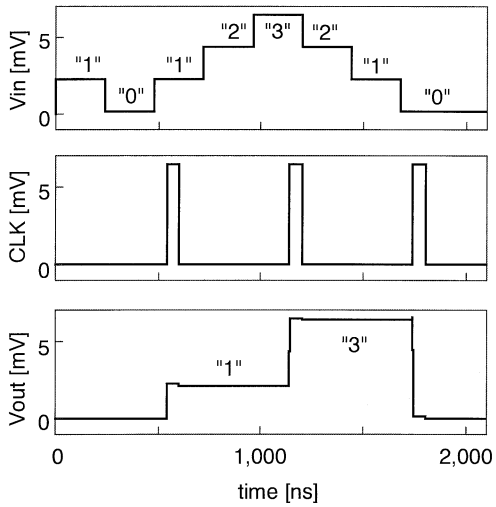


Fig. 7 Simulated D flip-flop operation for the circuit shown in Fig. 4.

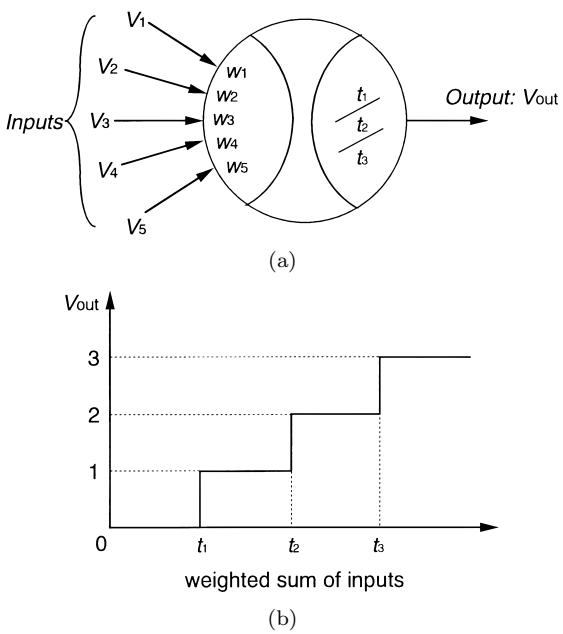


Fig. 8 Schematic diagrams of (a) the SET multiple-valued threshold device, and (b) its characteristic.

$$V_{out} = \begin{cases} 0 & \text{when} \quad \sum w_i \cdot V_i < t_1 \\ 1 & \text{when} \quad t_1 \le \sum w_i \cdot V_i < t_2 \\ 2 & \text{when} \quad t_2 \le \sum w_i \cdot V_i < t_3 \\ 3 & \text{when} \quad t_3 \le \sum w_i \cdot V_i < t_4, \end{cases} \tag{4}$$

where w_i indicates the weight of the input, and V_i indicates the input voltage. The weight w_i for each input and the threshold values t_i are specified for each use.

The SET inverter can be used to create a multiple-valued threshold device. For this purpose, we have to construct a sum-of-product unit for more than one input. It can be easily achieved by attaching input capacitors between the input nodes and the islands as shown in Fig. 9. The value of each capacitance is determined in such a way as to give a weighted connection for each input signal.

Using the threshold devices, any type of logic circuit can be constructed. Figure 10 shows an example: a full-adder circuit. Here, the parameter values are assumed as follows. The capacitances of the tunneling junctions are the same as previously described, i.e., $C_{j1} = 1\,\text{aF}$ and $C_{j2} = 2\,\text{aF}$. The other parameters are as follows.

For inverter 1,
the capacitance of input capacitors are 2 aF for all the inputs, $C_{B1} = 8.5\,\text{aF}$, $C_{L1} = 15\,\text{aF}$, and $V_{dd1} = 5.9\,\text{mV}$.

For inverter 2,

$$C_{G2} = 1\,\text{aF},\ C_{B2} = 20\,\text{aF},\ C_{L2} = 70\,\text{aF},\ \text{and}\ V_{dd2} = 3.6\,\text{mV}$$

For inverter 3,
the input capacitor for $\overline{carry}$ signal is 2.8 aF, other input capacitors are 2 aF. $C_{B3} = 7\,\text{aF}$, $C_{L3} = 75\,\text{aF}$, and $V_{dd3} = 6.4\,\text{mV}$.

For inverter 4,
the parameters are the same as those of the multiple-valued inverter, i.e.,

$$C_{G4} = 2\,\text{aF},\ C_{B4} = 10\,\text{aF},\ C_{L4} = 72\,\text{aF},\ \text{and}\ V_{dd4} = 6.5\,\text{mV}$$

The results of Monte-Carlo simulation of the adder circuit operation are summarized in Fig. 11. In the simulation, all the tunneling resistances were 1 MΩ. It can be seen that the simulated operation is correct for all combinations of quaternary values. The parameters are, however, not the optimized ones. The reliability is poor with these parameters. An error occurs when the output from inverter 1 is later than the transition of the state of inverter 3. One way to increase the reliability of the circuit is to increase the ratio of the tunneling resistances of inverter 1 to the tunneling resistances of inverter 3. Since the lower limit of the tunneling resistance is a few 100 kΩ [1], the resistance of the tunneling junction of inverter 3 must be much larger than 1 GΩ to make the full-adder circuit reliable. This method would decrease the response speed of the adder. While other ways to increase reliability should be investigated, we have shown that construction of a logic circuit is possible with this threshold device.

5. Implementation Issues

5.1 Thermal Error

The above description, in which the temperature is assumed to be 0 K, is not necessarily an accurate description of operation at non-zero temperature. We investigated the effect of thermal agitation by using a Monte

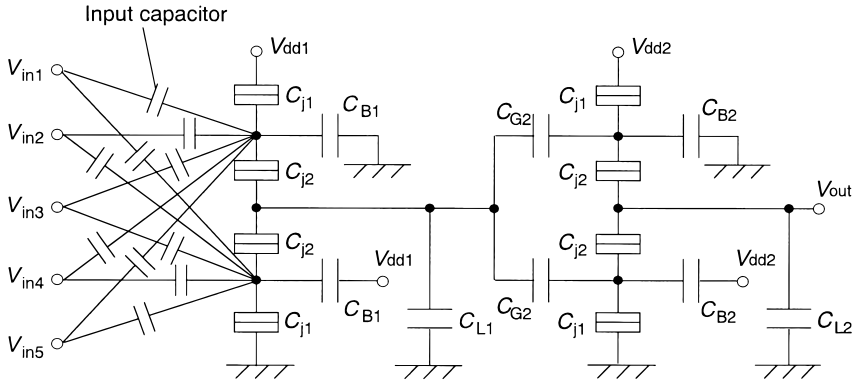


Fig. 9 Circuit construction of the SET multiple-valued threshold device circuit.

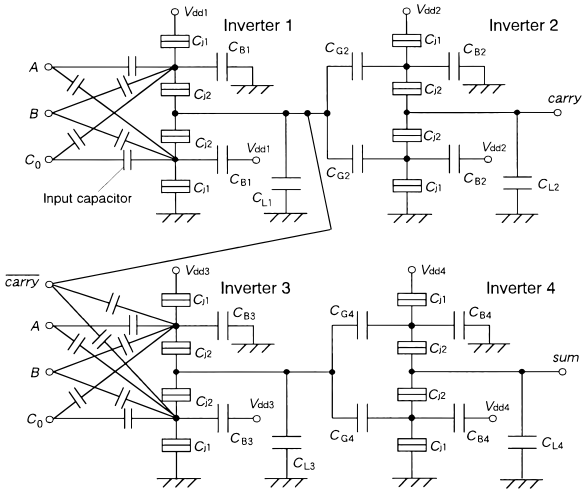


Fig. 10 Circuit diagram of an SET full adder circuit.

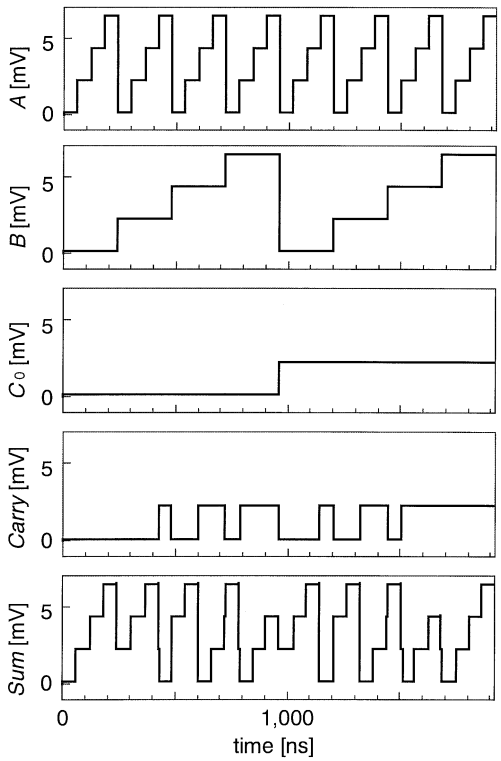


Fig. 11 Summary of the simulation results of operation of the SET full adder circuit. The temperature is assumed to be 0 K.

Carlo simulation of the circuit. We calculated the number of times there was a transition to an incorrect signal (number of errors) as well as the ratio of the total duration of each wrong output to the observation period (time ratio of errors). The input for the inverter was assumed to be fixed at 0.2 mV, and the errors were counted for when the internal state changed from $(0, -3, 0)$ to another state. We calculated the number of the errors and the time ratio of errors by observing the output signal for 60 ns. We repeated this procedure 100 times for different sets of random numbers and then calculated the mean value. The results are summarized in Fig. 12. Both quantities increase with temperature, and time ratio of errors reached 50% at 2 K. If the signal is binary and if we can judge the output signal value from the average of the output for a fixed period of time, the logic gate can be used at temperatures up to 2 K. However, the signal used in the test was a multiple-valued signal. Therefore, there is a possibility that the critical temperature for generating a multiple-valued signal is lower than 2 K. We simulated the averaged value of the output voltage during 10 μs at several temperatures. The result is shown in Fig. 13. If we require that the average voltage be able to be used as the input signal of the next gate, the inverter gate can be used up to 2 K. This operation temperature is not impractical.

5.2 Discrepancies in Parameters

Discrepancies in the capacitance parameters alter the stability condition and the device characteristics. In the proposed inverter circuit, a discrepancy of 2% in all the capacitance values is fatal. The parameters should be accurate within 1% in order to achieve the multiple-valued inverter function.

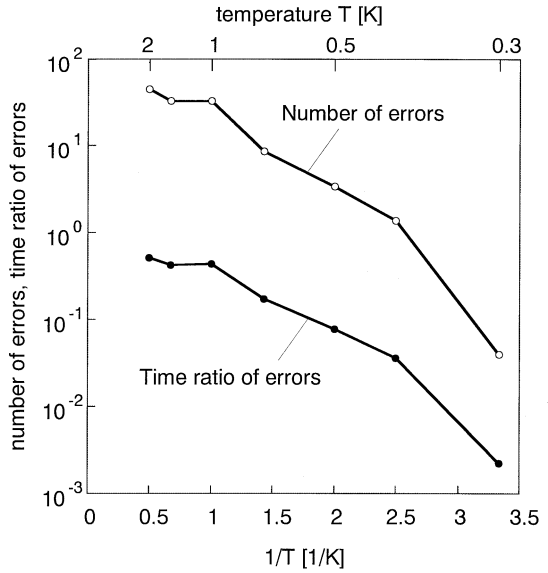


Fig. 12 The number of errors and the time ratio of errors in the output signal of the inverter.

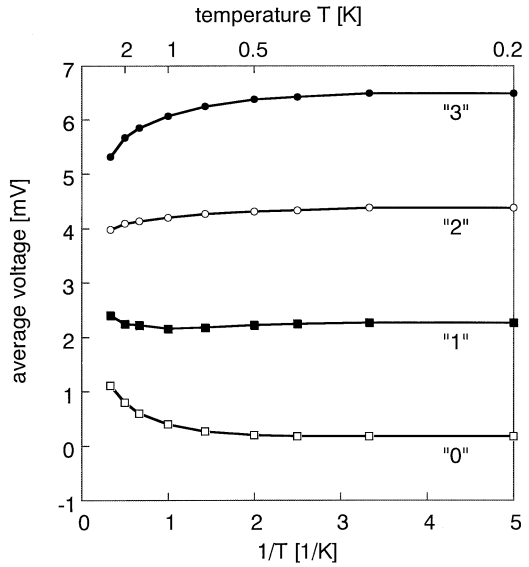


Fig. 13 Temperature dependence of the average of output voltage for 10 μs. The numbers indicate the corresponding multiple value.

Interconnection produces parasitic capacitance, which alters the load capacitance C_L. In the inverter operation, changing C_L modifies the output voltage. When the other parameters are exact, the maximum permissible discrepancy in C_L is ± 10 aF.

A discrepancy in V_{dd} causes a large hysteresis or bias condition that destroys the Coulomb blockade. Judging from the stability diagram shown in Fig. 2, the discrepancy of V_{dd} should be less than ± 0.1 mV.

5.3 Power Consumption

We can estimate the power consumption of the inverter circuit as follows. The maximum power consumption in an inverter gate can be estimated by the power consumption $P_{\max}$ by 3-electrons being charged and discharged in the load capacitance C_L by

$$P_{max} = \frac{(3e)^2}{C_L} f, \tag{5}$$

where e is the elementary charge, and f is the clock frequency. This equation gives a maximum power consumption of 2.7 fW for a clock operation with a 120 ns on-off period. This value is much smaller than typical values for CMOS MVL gates, which usually range between μW and mW.

The fabrication of the proposed device is difficult using present technology, but the results of this investigation have shown that it is physically possible for SET circuits to generate, transfer and hold multiple-valued signals.

6. Conclusion

We proposed a SET inverter circuit for a multiple-valued logic circuit. The circuit consists of only two SET transistors. The circuit performs both the inverter function for a multiple-valued logic circuit and the memory function. A quantizing circuit and a D flip-flop circuit can be constructed by combining two inverters. A threshold device that uses the inverter was also proposed. A full adder circuit can be constructed by using only two threshold devices. Implementation issues were also discussed.

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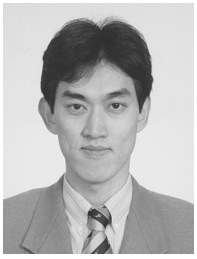
References

[1] H. Grabert and M.H. Devoret, Single Charge Tunneling—Coulomb Blockade Phenomena in Nanostructures, Plenum Press, New York, 1992.
[2] T. Higuchi and M. Kameyama, Multiple-Valued Digital Processing Systems, Syoukoudou, 1989, and references therein.
[3] T. Hanyu, M. Kameyama, and T. Higuchi, "Prospects of multiple-valued VLSI processors," IEICE Trans. Electron., vol.E76-C, no.3, pp.383–392, 1993.
[4] A.J. McAuley, "Four state asynchronous architectures," IEEE Trans. Comput., vol.41, no.2, pp.129–142, 1992.

[5] J.R. Tucker, "Complementary digital logic based on the 'Coulomb blockade'," J. Appl. Phys., vol.72, pp.4399–4413, 1992.
[6] N. Kuwamura, K. Taniguchi, and C. Hamaguchi, "Simulation of single electron logic circuits," IEICE Trans., vol.J77-C-II, no.5, pp.221–228, 1994.
[7] M. Akazawa and Y. Amemiya, "Eliciting the potential functions of single-electron circuits," IEICE Trans. Electron., vol.E80-C, no.7, pp.849–858, 1997.
[8] N. Asahi, M. Akazawa, and Y. Amemiya, "Single-electron logic device based on the binary decision diagram," IEEE Trans. Electron Devices, vol.44, no.7, pp.1109–1116, 1997.



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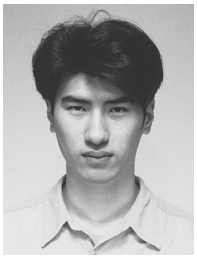

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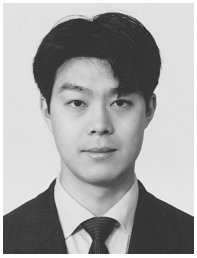

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