ELectronics EXpress

IEICE Electronics Express, Vol.1, No.9, 248–252

Reaction-diffusion chip implementing excitable lattices with multiple-valued cellular automata

Hiroshi Matsubara,[a)] **Tetsuya Asai, Tetsuya Hirose, and Yoshihito Amemiya**

Graduate School of Information Science and Technology, Hokkaido University, Kita 13, Nishi 8, Kita-ku, Sapporo, Hokkaido, 060–8628 Japan

a) *asai@sapiens-ei.eng.hokudai.ac.jp*

Abstract: We designed a special CMOS circuit for reaction-diffusion computers that accepts optical inputs in parallel and generates excitable spatial waves on a chip surface. We demonstrated the spatiotemporal properties of the proposed circuits by fabricated LSIs.

Keywords: reaction diffusion system, reaction-diffusion chip, cellular automata, excitable lattice

Classification: Integrated circuits

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1 Introduction

Reaction-diffusion (RD) computers can be expected as a driving force that can develop analog computing technology to overcome the limits of present Neumann computing architectures [1]. Challenges to this promising area have already been reported by several pioneers. For example, optimal path planning, skeltonization of binary images, and path planning for robot navigation—all of which are intractable for Neumann computing— can effectively be performed by means of chemical RD systems (see overview in [1, 2]). In these examples, spatiotemporal dynamics of chemical waves represent in-

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DOI: 10.1587/elex.1.248
Received July 14, 2004
Accepted July 16, 2004
Published August 10, 2004

formation and process the information quickly in a sophisticated, parallel manner. However, when it comes to putting chemical RD systems into practice, we will encounter serious problems such as unportability (chemistry apparatus are large and fragile) and low speed operation (chemical waves travel very slowly). To overcome these problems, we proposed and fabricated semiconductor RD computing devices (RD chips) that implemented RD dynamics [3, 4]. The prototype chips exhibited animated spatiotemporal dynamics as observed in chemical RD systems [4] and, unlike the chemical systems, were easy to control their temporal dynamics [3]. However, the unit cell circuit we used in these prototype chips were not small enough to implement large RD systems that we can use for practical information processing. In this paper, we propose an concise cell circuit that can construct large electrical RD systems in a chip. The cell circuit we propose is designed on the basis of a multiple-valued cellular automata (CA) model, called *excitable lattices* [1]. Using this cell circuit, we design an RD chip that can accept parallel optical inputs, which is very useful for parallel image-processing applications.

2 Excitable-Lattice CA Model and its CMOS circuit

The excitable lattice [1] is a CA model in which each cell is regularly arranged on a 2-D grid. Each cell has eight neighbors and each cell state is updated in a discreet time step, as in conventional CA. The CA model has a multiple-valued state variable, and takes excitatory (EXC), refractory (REF), and resting (RES) states. Figure 1 (a) shows the state diagram. The dynamics are given by

$$x^{t+1} = \begin{cases} \mathrm{EXC}\,, & (x^t = \mathrm{RES}) \wedge (s^t(x) \geq 1) \\ \mathrm{REF}\,, & (x^t = \mathrm{EXC}) \\ \mathrm{RES}\,, & (x^t = \mathrm{RES}) \wedge (s^t(x) = 0) \vee (x^t = \mathrm{REF}) \end{cases}, \tag{1}$$

where $s^t(x)$ is the number of excitatory cells among the neighbors, x^t and x^{t+1} represent a cell's current and subsequent states, respectively. A cell becomes excited when it is in the resting state and the number of excitatory cells among its neighbors is larger than 1. Then, the states changes from excitatory to refractory state in the subsequent step. Next, the state is changed from the refractory to the resting state. A cell is stable in its resting state as long as the number of excitatory cells among the cell's neighbors is zero.

The excitable lattice mimics fundamental spatiotemporal properties of the BZ system, i.e., excitable wave propagation and annihilation, on the lattices. Figure 1 (b) illustrates examples of the lattice's operation. At an initial state (step 0), two corner cells ($\circ$) are excited and remaining cells are resting ($\bullet$). At step 1, neighboring cells of the two corner cells are also excited ($\circ$) and the state of the corner cells are changed from excitatory to refractory state ($\star$). Other cells are still in their resting states ($\bullet$) at this step. At step 2, resting cells being next to excitatory cells are excited likewise ($\circ$), and states of the corner cells are changed from refractory to resting state ($\bullet$).

© IEICE 2004
DOI: 10.1587/elex.1.248
Received July 14, 2004
Accepted July 16, 2004
Published August 10, 2004

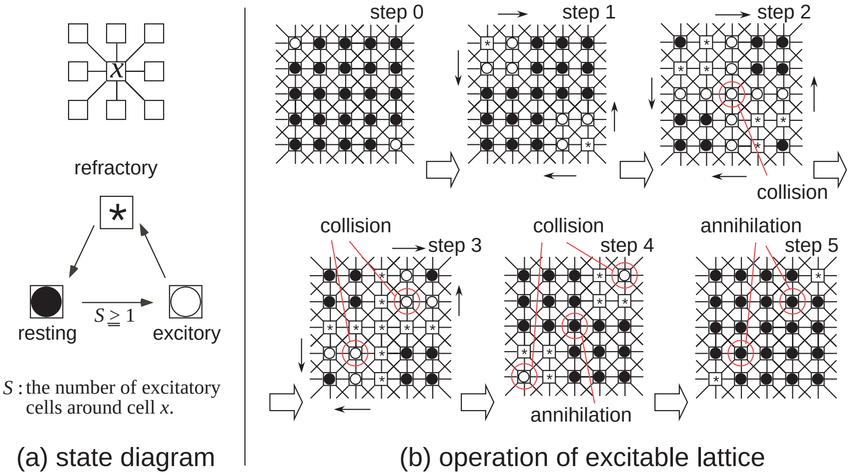


Fig. 1. Excitable lattice model.

Consequently, excitatory waves whose wave fronts are represented by groups of excitatory cells (∘) propagate on the lattice. At this step, two excitatory waves generated by the two corner cells collide at the center of the lattice (∘). At step 3, since neighboring cells of the center cell along the direction of the excitatory waves, are resting (•) or in refractory state (⋆), no waves propagate in this direction and the state of the center cell is changed from excitatory to refractory (⋆). This cell's state is further changed from refractory to resting states (•) at step 4. Consequently, the wave front disappears at this center cell. Likewise, excitatory waves on this lattice disappear at any location at which they collide.

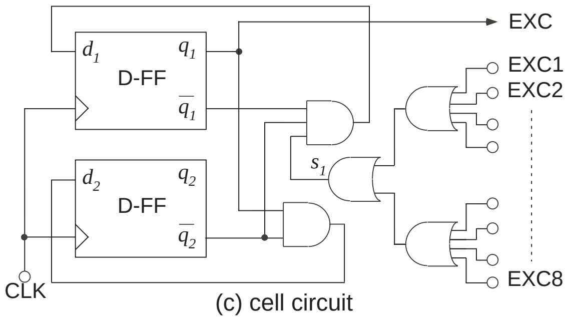
MSB	LSB	state
1	0	EXC
0	1	REF
0	0	RES

(a) binary state

true if $S \geqq 1$ / current state / subsequent state

s_1	$(q_1,$	$q_2)$	$(d_1,$	$d_2)$	transition
1	0	0	1	0	RES → EXC
x	1	0	0	1	EXC → REF
x	0	1	0	0	REF → RES
0	0	0	0	0	RES → RES

(b) binary transition rule



(c) cell circuit

Fig. 2. Binary cell circuit.

We implement this excitable lattice using standard CMOS circuits. Since a cell has three states, we represent the cell state by 2-bit binary values, as shown in Fig. 2(a). The cell dynamics in (1) are therefore represented by a binary transition rule [Fig. 2 (b)] where (q_1, q_2) and (d_1, d_2) represent a

© IEICE 2004
DOI: 10.1587/elex.1.248
Received July 14, 2004
Accepted July 16, 2004
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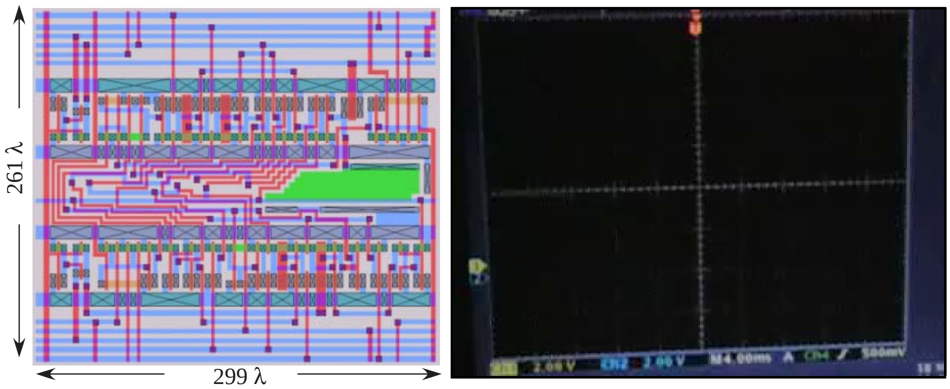
IEICE Electronics Express, Vol.1, No.9, 248–252

cell's current and subsequent states, respectively, and s_1 is logical "1" when the number of excitatory cells among the cell's neighbors is larger than 1. Otherwise, s_1 is logical "0". From Fig. 2 (b), we obtain

$$d_1 = s_1 \bar{q}_1 \bar{q}_2, \quad d_2 = q_1 \bar{q}_2. \tag{2}$$

Figure 2 (c) illustrates the resulting cell circuit. Logic functions given by Eq. (2) are implemented by using NAND gates. To store the cell state (d_1, d_2), we employ two D-type flipflops (D-FFs) *per* cell circuit. Since Fig. 2 (b) indicates that q_1 of each cell is logical "1" only when the cell is excited, the output EXC of each cell can be represented by q_1. Now s_1 is obtained by logical OR operation of output EXC (q_1) of each cell's eight neighbors.



(a) Layout of cell circuit (b) Recorded excitable waves

Fig. 3. Cell layout and recorded results (in movie).

3 Experimental Results

We fabricated a proposed RD chip that implements 16×16 cells using 1.5-μm double-poly double-metal n-well CMOS process (MOSIS, Vendor: AMIS). Figure 3 (a) shows the layout of a cell circuit, including a photo detector (green area: simple pn junction between p-substrate and n-diffusion) and additional switching circuits for reset and readout operations. All circuit areas except for photodetectors were masked by top metal. The resulting cell size was $261\lambda \times 299\ \lambda$ ($\lambda = 0.8\,\mu$m).

We recorded spatiotemporal patterns of the fabricated RD chip with the following readout circuitry. Each cell in the chip was located beneath each wire crossing row and column buses, and was connected to a common-output wire through a transfer gate. The gate connects the cell's output to the common wire when both the row and column buses are active. Thus a cell's output (EXC) appeared on the common output wire when the cell was selected by activating the corresponding row and column buses simultaneously. We could obtain a binary stream from the common output wire by selecting each cell sequentially. Using a conventional displaying technique, the binary stream was reconstructed on a 2-D display. Figure 3 (b) shows the movie we

© IEICE 2004
DOI: 10.1587/elex.1.248
Received July 14, 2004
Accepted July 16, 2004
Published August 10, 2004

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recorded. Each yellow dot represents an excitatory cell where EXC is logical "1". In the experiment, the supply voltage were set at 5 V, and the system clock was set at low frequency (2.5 Hz) so that "very-slow" spatiotemporal activities could be observed visually (the low frequency was used only for the visualization, and was not the upper limit of the circuit operation). We applied pin-spot lights to several cells at top-left and bottom right corners of the chip. The circuit exhibited the expected results; i.e., two excitable waves of excited cells triggered by the corner cells propagated toward the center and disappeared when they collided. This result suggests that if we use a more microscopic process and a large number of cells were implemented, we would observe the same complex (BZ-like) patterns, as observed in the original excitable lattices [1].

4 Conclusion

We fabricated a reaction-diffusion (RD) chip based on a multiple-valued cellular-automaton (CA) model of excitable lattices. Our experiments confirmed the expected operations, i.e., excitable wave propagation and annihilation. The chip can operate much faster than real chemical RD systems, even when the system clock frequency is $O(1)$ Hz, and is much easier to use in various experimental environments. Therefore, the chip should encourage RD application developers who use such properties of excitable waves to develop unconventional computing schemes, e.g., chemical image processing, pattern recognition, path planing, and robot navigation.

Acknowledgments

The authors wish to thank Professor Andrew Adamatzky of the University of the West of England for most valuable discussions and suggestions during the research.

© IEICE 2004
DOI: 10.1587/elex.1.248
Received July 14, 2004
Accepted July 16, 2004
Published August 10, 2004