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Power-supply circuits for ultralow-power subthreshold MOS-LSIs

Tetsuya Hirose[a)], **Tetsuya Asai, and Yoshihito Amemiya**

Department of Electrical Engineering, Hokkaido University

Kita 14, Nishi 9, Sapporo 060–0814, Japan

a)*hirose@sapiens-ei.eng.hokudai.ac.jp*

Abstract: A low-voltage power supply circuit is developed for micropower CMOS LSI applications, especially for microwatt smart-sensor LSIs. The circuit consists of a switched-capacitor voltage converter and a series regulator. The switched converter lowers battery voltage 1.5–3 V to a low voltage of 0.5–0.7 V to drive the series regulator, and the series regulator provides LSI logic gates with a power voltage of 0.4–0.6 V such that the logic gates operate in the subthreshold region. In a sample circuit designed to produce a supply voltage of 0.6 V, the switched converter lowered a 1.5-V battery voltage to 0.68 V, and the series regulator lowered the 0.68 V to 0.6 V. The power conversion efficiency of the switched converter was 83%, and the total efficiency was 73%, with a 13-μA output current.

Keywords: ultralow-power, subthreshold LSI, power supply circuit, switched-capacitor converter, series regulator

Classification: Integrated circuits

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1 Introduction

In the near future, new social information infrastructures, or "ubiquitous" network systems, will be developed to provide promising communication platforms for collecting and delivering information throughout the world. Such systems will need a huge number of distributed smart sensor LSIs to measure various physical data in our surroundings, store and process the measured data, and output the data on demand (see [1, 2] for an example of such sensors). Figure 1-(a) depicts the architecture of such smart sensor LSIs. These sensor LSIs must operate with low power dissipation —at a microwatts level or less— because they will probably be used under conditions where they have to draw necessary energy from microbatteries or from other poor, less-than-ideal power sources.

To achieve microwatt operation, logic gates in the processors and memories have to be operated in the subthreshold (or weak-inversion) region of MOSFETs. This requires that logic gates be driven with a low voltage of about 0.4–0.6 V. However, the external supply voltage that is available is far higher than desired: about 1.5 V for manganese batteries and 3 V for lithium ones. Therefore, an on-chip DC–DC voltage converter is needed to lower the battery voltage to 0.4–0.6 V with high efficiency. However, ordinary voltage converters are unsuitable for our purpose because they are designed for high-power, milliwatt or larger power applications and cannot operate efficiently in the microwatt regions [3, 4, 5, 6]. For subthreshold-operated LSIs, we developed a power-supply circuit consisting of a low-voltage DC–DC converter and a series regulator specialized for microwatt operation. The details of this circuit are described in the following sections.

2 Circuit Configuration

The configuration of our power-supply circuit is depicted in Fig. 1-(b). The circuit consists of a switched-capacitor (SC) converter and a series regulator. The SC converter lowers external battery voltage V_{IN} to an intermediate low voltage V_{LL}. The series regulator accepts V_{LL} and produces an appropriate supply voltage V_{OUT} such that connected LSI logic gates operate in a subthreshold region.

The SC converter is based on the method of SC voltage dividing [6, 7]. Ordinary SC converters use a single divider (capacitors C_1 and C_2 and four switches) to lower its input voltage. In our circuit, however, we added a complementary divider (capacitors C_3 and C_4 and four more switches) to achieve high conversion efficiency in low-current, microwatt operation. The

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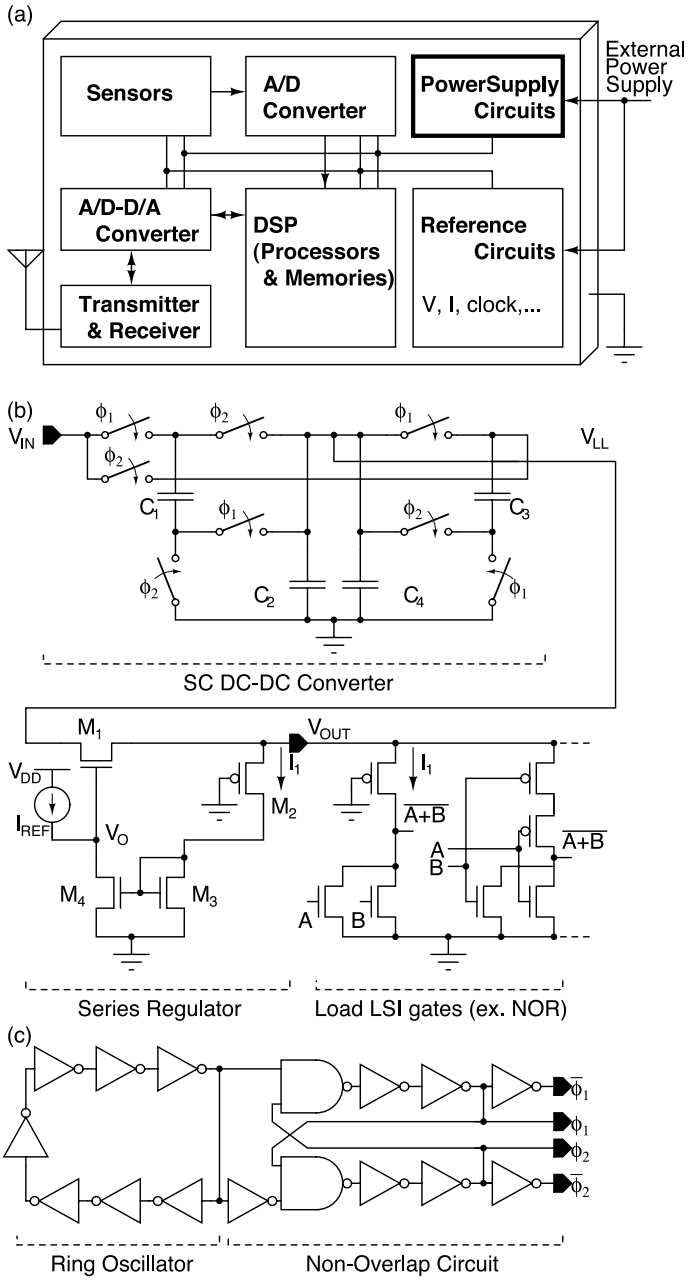

Fig. 1. (a) Chip architecture of microwatt smart-sensor LSIs, and power-supply circuits: (b) SC converter and Series Regulator, and (c) clock generator.

two dividers are driven complimentarily with clocks ϕ_1 and ϕ_2.

The series regulator is controlled by reference current I_{REF} to produce output V_{OUT} such that current I_1 in a monitoring transistor M_2 is equal to I_{REF}. This is performed through negative feedback: $V_{OUT} \rightarrow I_1 \rightarrow$ current in $M_4 \rightarrow V_O \rightarrow$ resistance of M1 $\rightarrow V_{OUT}$. With this regulation, the supply current through each LSI gate is limited to reference current I_{REF}. By setting I_{REF} to 1–10 nA, we can operate the logic gates in the subthreshold region with an appropriate supply voltage.

Clocks ϕ_1 and ϕ_2 for the SC converter have to be reverse-phased and non-overlapping. Figure 1-(c) shows the clock generator for this purpose; it

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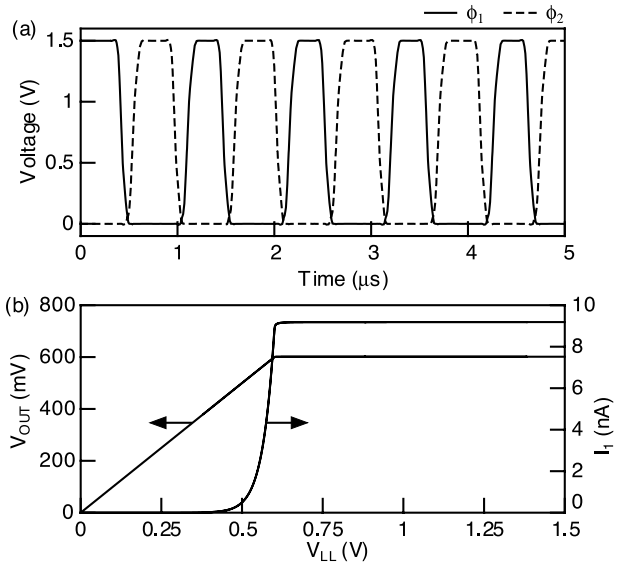

Fig. 2. Characteristics of (a) clock generator — waveforms of clocks ϕ_1 and ϕ_2, and (b) series regulator — output V_{OUT} and monitored current I_1 as a function of input V_{LL}.

consists of a ring oscillator and a non-overlapping subcircuit. To limit power consumption, we constructed the clock generator with the current-starved NAND gates and inverters.

3 Simulation Results

We designed a sample circuit, assumed a set of 0.35-μm standard CMOS parameters and a 1.5-V battery voltage, and confirmed the operation of the circuit with SPICE simulation.

Figure 2-(a) shows the waveforms of non-overlapping clocks ϕ_1 and ϕ_2, with the oscillation frequency of 950 kHz. The power consumption of the clock generator was 0.75 μW. Figure 2-(b) plots the transfer curves of the series regulator, i.e., output V_{OUT} and monitored current I_1 (see Fig. 1-(a)) as a function of input V_{LL}. The reference current I_{REF} was set at 10 nA. The circuit operated successfully at the V_{LL} of 0.6 V or higher.

The waveforms of V_{LL} (SC converter output) and V_{OUT} (series regulator output) are plotted in Fig. 3-(a), with capacitances $C_1 = C_2 = C_3 = C_4 = = 50$ pF, $I_{REF} = 10$ nA, and output current (load current) = 13 μA. The average and the ripple were 0.68 V and 40 mV_{pp} for V_{LL}, and 0.60 V and 5 mV_{pp} for V_{OUT}. Figure 3-(b) plots the efficiency of the SC converter, which include the power of the clock generation circuit, and Fig. 3-(c) shows the average and the ripple of V_{LL} as a function of the output current, with the capacitance as a parameter. With the capacitance of 50 pF, the SC converter and the total circuit showed a maximum power conversion efficiency of 83%, and 73%, respectively, at 13-μA output current. The output V_{LL} decreased, and the ripple ΔV_{LL} increased with the load current. This can be improved by using a larger value of the capacitance; a larger capacitance needs a larger

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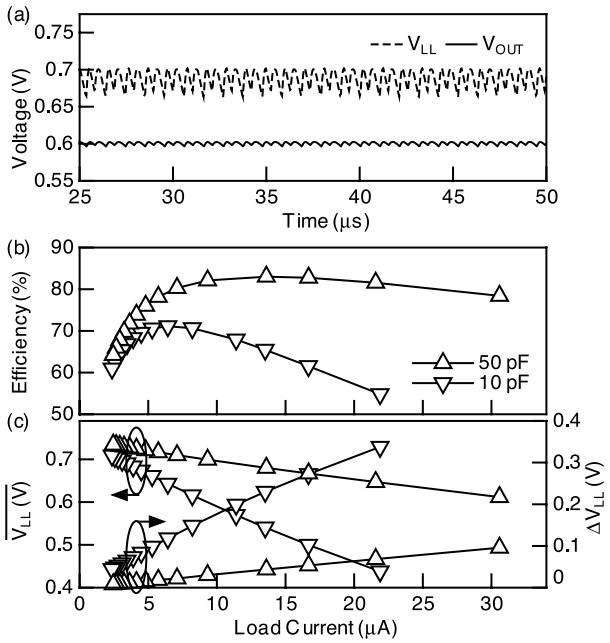

Fig. 3. Operation of the total circuit: (a) waveforms of V_{LL} (SC converter output) and V_{OUT} (series regulator output); (b) efficiency of the SC converter as a function of output current; and (c) average $\overline{V_{LL}}$ and ripple ΔV_{LL} as a function of output current.

area but can be implemented on the periphery of the chip. With these results, we will be able to develop subthreshold-operated LSIs including microwatt smart-sensor LSIs.

4 Conclusion

We developed an on-chip high-efficiency switched capacitor DC–DC voltage converter and series regulator for ultralow-power subthreshold MOS LSIs. The circuit operation was confirmed by the 0.35 μm standard CMOS process. Simulation results of the circuits have shown that the power conversion efficiency of the SC DC–DC converter and the total circuit are 83% at voltage V_{LL} of 0.68 V, and 73% at voltage V_{OUT} of 0.6 V, respectively, with a 13-μA load current, and that series regulator can operate at a low power supply of 0.6 V with 10 nA reference current. The circuit can be used as a power supply circuits for the subthreshold CMOS digital circuits.

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