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Temperature-compensated CMOS current reference circuit for ultralow-power subthreshold LSIs

Tetsuya Hirose[a)], **Tetsuya Asai, and Yoshihito Amemiya**

Department of Electrical Engineering, Hokkaido University,
Kita 14, Nishi 9, Sapporo 060–0814, Japan

a) *hirose@sapiens-ei.eng.hokudai.ac.jp*

Abstract: This paper proposes a low-current reference circuit for power-aware LSI applications. The circuit consists of two current generation subcircuits which are based on β-multiplier circuit, one with a positive and the other with a negative temperature coefficient. The variation of the reference current in a sample circuit designed to produce a current of 230 nA can be kept very small within $\pm 1.3\%$ in a wide temperature range of -20 to 100°C.

Keywords: power-aware LSI, subthreshold LSI, MOSFET, subthreshold region, current reference circuit

Classification: Integrated circuits

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1 Introduction

In the near future, a new social information infrastructures, or "ubiquitous" network systems, will make it possible to collect and deliver information

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throughout the world. In such systems, numerous distributed smart sensors will measure various physical data in our surroundings, store and process the measured data, and output the data on demand. The sensor LSIs must be able to operate with ultralow power because they will probably be powered by microbatteries or will be placed in less-than-ideal surroundings with poor sunshine, weak electric waves, or slight differences in temperature between day and night. To create such an ultralow-power LSI, we have designed a circuit that operates in the subthreshold region of MOSFETs. For LSIs operated in this region, we first need to develop a constant reference current circuit as an elementary circuit block with ultralow power dissipation.

For ultralow-power operation, reference circuits operating with nanoampere-order current have been reported [1, 2]. However, the circuit configuration is quite complex and uses a large number of MOS transistors, and the circuits require a digital trimming technique. Therefore, it is difficult to ensure stable operation and low cost of sensor LSIs. The simple CMOS current reference circuit proposed by Oguey and Aebischer generates a small output current [3]. However, because the output current increases as the temperature increases, the circuit can not be used as a reference current circuit in an environment where the temperature changes. Although the circuit itself can not be used as a reference current circuit, a current reference circuit with little temperature dependence can be constructed by developing a circuit whose output current decreases with temperature. In this work, we constructed a current subcircuit that shows negative temperature dependence and, by combining it with Oguey's circuit, developed a current reference circuit specialized for ultralow-power subthreshold LSIs. The details of this circuit are described in the following sections.

2 Circuit configuration

2.1 Operation principle

The current reference circuit consists of a positive temperature coefficient (PTC) current generation subcircuit [3], a negative temperature coefficient (NTC) current generation subcircuit, and a current adder subcircuit, as shown in Fig. 1. The PTC and NTC subcircuits generate currents I_{PTC} and I_{NTC}, which have positive and negative temperature dependence, respectively. The current adder subcircuit accepts the currents and generates a reference current I_{REF} with little temperature dependence.

Except for the transistors used as MOS resistors (M_{R1} and M_{R2}) and bias voltage generator (M_{B1} and M_{B2}), all MOSFETs are operated in the subthreshold region. The difference between the PTC and NTC subcircuits is the bias voltage generation method for the MOS resistors. In the PTC subcircuit, bias voltage V_{B1} for MOS resistor M_{R1} is generated by the diode-connected transistor M_{B1} operated in the strong-inversion region, whereas, in the NTC subcircuit, bias voltage V_{B2} for MOS resistor M_{R2} is generated by two diode-connected transistors in a cascode connection: transistor M_{B2} is operated in the strong-inversion region and M_{B3} in the subthreshold region.

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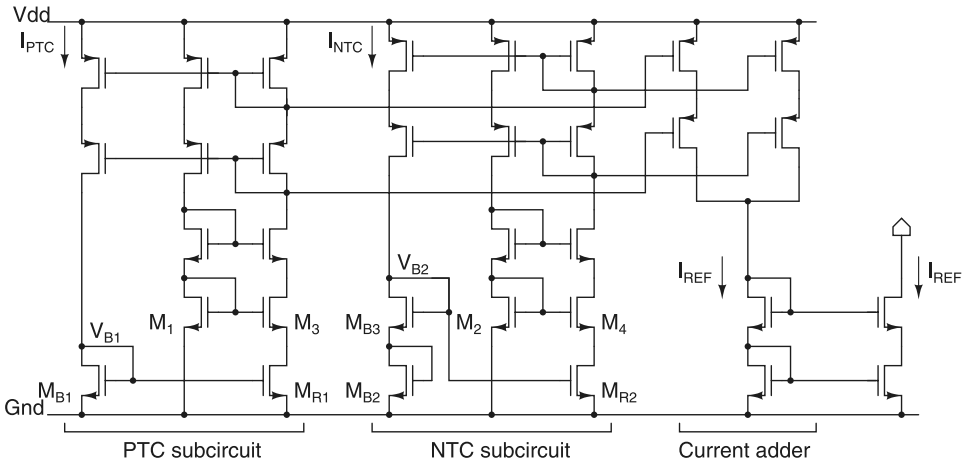

Fig. 1. Circuit configuration.

The temperature dependence of bias voltage V_{B2} in the NTC subcircuit is larger than that of bias voltage V_{B1} in the PTC subcircuit. Therefore, by exploiting the temperature characteristics of bias voltages, the currents can be made to have different temperature characteristics. In the case of the PTC subcircuit, because reduction of threshold voltage V_{TH} with temperature makes the temperature dependence of current I_{PTC} positive. On the other hand, in the case of the NTC subcircuit, because the temperature dependence of bias voltage V_{B2} becomes larger than that of threshold voltage V_{TH}, current I_{NTC} has negative temperature dependence. In the following, the details of the circuit operation and the temperature dependence of the currents are described.

2.2 Temperature dependence

The PTC and NTC subcircuits we designed are based on the β-multiplier self-biasing circuit [4] and use MOS resistors with different bias voltages (V_{B1} and V_{B2}) instead of a resistor. Although bias voltage generation methods are different, the temperature characteristics of the currents can be analyzed in the same manner because the circuit configurations in PTC ($\mathrm{M}_1-\mathrm{M}_3-\mathrm{M}_{\mathrm{R1}}$) and NTC ($\mathrm{M}_2-\mathrm{M}_4-\mathrm{M}_{\mathrm{R2}}$) are the same, as shown in Fig. 1.

The subthreshold MOS current for a drain-source voltage V_{DS} higher than 0.1 V is given by

$$I = KI_0 \exp\left(\frac{V_{GS}-V_{TH}}{\eta V_T}\right) , \tag{1}$$

where $I_0(=\mu C_{OX} V_T^2 (\eta-1))$ is called the pre-exponential factor, K is the aspect ratio, μ is the mobility, C_{OX} is the gate-oxide capacitance, V_T is the thermal voltage, η is the subthreshold swing parameter, and V_{TH} is the threshold voltage.

In the circuit in Fig. 1, the gate-source voltage $V_{GS,i}$ $(i=1,2)$ in M_i must be equal to the sum of the gate-source voltage $V_{GS,i+2}$ in M_{i+2} and the drain-source voltage $V_{DS,Ri}$ in $\mathrm{M}_{\mathrm{R}i}$, or

$$V_{GS,i} = V_{GS,i+2} + V_{DS,Ri} \quad (i=1,2) . \tag{2}$$

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Because the current I through the transistors M_i and M_{i+2} are the same, Eq. (2) can be rewritten as

$$V_{DS,Ri} = \eta V_T \ln\left(\frac{K_{i+2}}{K_i}\right) , \tag{3}$$

where K_i and K_{i+2} are the aspect ratios of transistors M_i and M_{i+2}. For a given bias voltage V_{Bi}, the current I in the circuit is expressed by

$$I = \beta_R \left(V_{Bi} - V_{TH}\right) V_{DS,Ri} . \tag{4}$$

The temperature dependences of the threshold voltage V_{TH} and mobility μ are $V_{TH}(T) = V_{TH0} - \kappa T$ and $\mu(T) = \mu(T_0)(T/T_0)^{-m}$, respectively, where V_{TH0} is the threshold voltage at the absolute zero temperature, κ is the temperature dependence parameter of the threshold voltage, $\mu(T_0)$ is the carrier mobility at room temperature T_0, and m is the mobility temperature exponent. The temperature coefficient of the current $TC_I (= \frac{1}{I}\frac{dI}{dT})$ can be expressed by

$$\begin{aligned} TC_I &= \frac{1}{\beta_R}\frac{d\beta_R}{dT} + \frac{1}{V_{Bi} - V_{TH}}\frac{d\left(V_{Bi} - V_{TH}\right)}{dT} + \frac{1}{V_{DS,Ri}}\frac{dV_{DS,Ri}}{dT} \\ &= \frac{1-m}{T} + \frac{1}{V_{Bi} - V_{TH}}\frac{d\left(V_{Bi} - V_{TH}\right)}{dT} . \end{aligned} \tag{5}$$

Because the value of m is about 1.5 for ordinary MOSFETs, the first term of Eq. (5) becomes a negative value. However, by changing the temperature dependence of bias voltage V_{Bi} in the second term, TC_I can be made a positive or negative value.

In the PTC subcircuit, bias voltage V_{B1} for MOS resistor M_{R1} is generated by the diode-connected transistor M_{B1} operated in the strong-inversion region. The voltage V_{B1} can be given by

$$V_{B1} = V_{TH} + \sqrt{\frac{2I_{PTC}}{\beta}} . \tag{6}$$

From Eqs. (5) and (6), TC_I in the PTC subcircuit can be expressed by

$$TC_I = \frac{2-m}{T} \tag{7}$$

As mentioned above, because the value of m is about 1.5, TC_I in the circuit is always positive, and current I_{PTC} will increase as the temperature increases.

In the NTC subcircuit, bias voltage V_{B2} for MOS resistor M_{R2} is generated by two diode-connected transistors. We operate transistors M_{B2} and M_{B3} in the strong-inversion region and in the subthreshold region, respectively. The voltage V_{B2} can be given by

$$V_{B2} = 2V_{TH} + \sqrt{\frac{2I_{NTC}}{\beta}} + \eta V_T \ln\left(\frac{I_{NTC}}{KI_0}\right) . \tag{8}$$

For simplicity, the body effect of transistor M_{B3} is not taken into account. From Eqs. (5) and (8), TC_I in the NTC subcircuit can be expressed by

$$TC_I = \frac{2-m}{T} - \frac{1}{T\left(1 - \frac{\kappa T - V_A}{V_{TH0}}\right)} \tag{9}$$

$$V_A = \frac{1}{2}\sqrt{\frac{2I_{NTC}}{\beta}} + \eta V_T \ln\left(\frac{I_{NTC}}{KI_0}\right) - \eta V_T \tag{10}$$

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In standard CMOS process parameters, voltage of V_A in Eqs. (9) and (10) becomes a very small value compared to κT and can be ignored for the first-order approximation. Moreover, because voltage V_{TH0} is sufficiently larger than κT ($V_{TH0} \gg \kappa T$), Eq. (9) can be rewritten as

$$TC_I = \frac{2-m}{T} - \frac{1}{T}\left(1 + \frac{\kappa T}{V_{TH0}}\right) = \frac{1-m}{T} - \frac{\kappa}{V_{TH0}} \,. \tag{11}$$

Therefore, TC_I in the circuit is negative, and current I_{NTC} will decrease as the temperature increases.

3 Results

Assuming a set of 0.35-μm standard CMOS process parameters and a 2.5-V power supply voltage, we designed a sample circuit to produce a current of 230 nA and confirmed its operation by SPICE simulation. In the simulations, the ratios K_3/K_1 and K_4/K_2 were set to 1.2 and 1.1, respectively. The simulations were performed on the typical process condition. Figure 2 (a) shows the simulated results for the output current I_{REF} for the circuit. PTC and NTC currents (I_{PTC} and I_{NTC}) are also plotted in the figure. The PTC and NTC currents increased and decreased with temperature, respectively, as expected. From the currents, temperature-compensated reference current I_{REF} can be obtained. The variation in the current $\Delta I_{REF}/\overline{I_{REF}}$ can be suppressed to within $\pm 1.3\%$ in the temperature range from -20 to 100°C. Figure 2 (b) shows the reference current as a function of the supply voltage. The circuit can operate at a low voltage of 1.7 V. The variation in the reference current can be suppressed to within 1.4% in the power supply voltage range from 1.7 to 3.3 V. The minimum supply voltage of 1.7 V can be reduced by using an operational amplifier instead of cascode current mirror configurations [4].

To verify the stability of the circuit operation, we performed a process corner analysis using parameters provided by the manufacturer. Process corners of NMOS and PMOS devices such as slow (S), typical (T) and fast (F), were considered in the simulations. Figure 3 shows the simulated characteristics of reference current I_{REF} under five different process corner conditions. Absolute values of I_{REF} changed with process corners. This is because the process corners of NMOS devices affect the current level through bias voltage V_{Bi}. At the slow (S) corner, because threshold voltage V_{TH} of NMOS becomes higher, bias voltage V_{Bi} also increases. The increase of bias voltage V_{Bi} decreases the resistance in MOS resistors. Therefore, the reference current level increases at slow process corner conditions. However, although the reference current level changes, reference current I_{REF} has little temperature dependence in each process corner condition. This is because TC_I of the PTC and NTC subcircuits stays almost constant for every process corner condition. This can be seen in Eqs. (7) and (11). From Eq. (7), TC_I of the PTC subcircuit depends on only mobility temperature exponent factor m. The value of m changes little with process corner conditions [6]. From Eq. (11), TC_I of the NTC subcircuit depends on m, κ, and V_{TH0}. Threshold voltage at absolute

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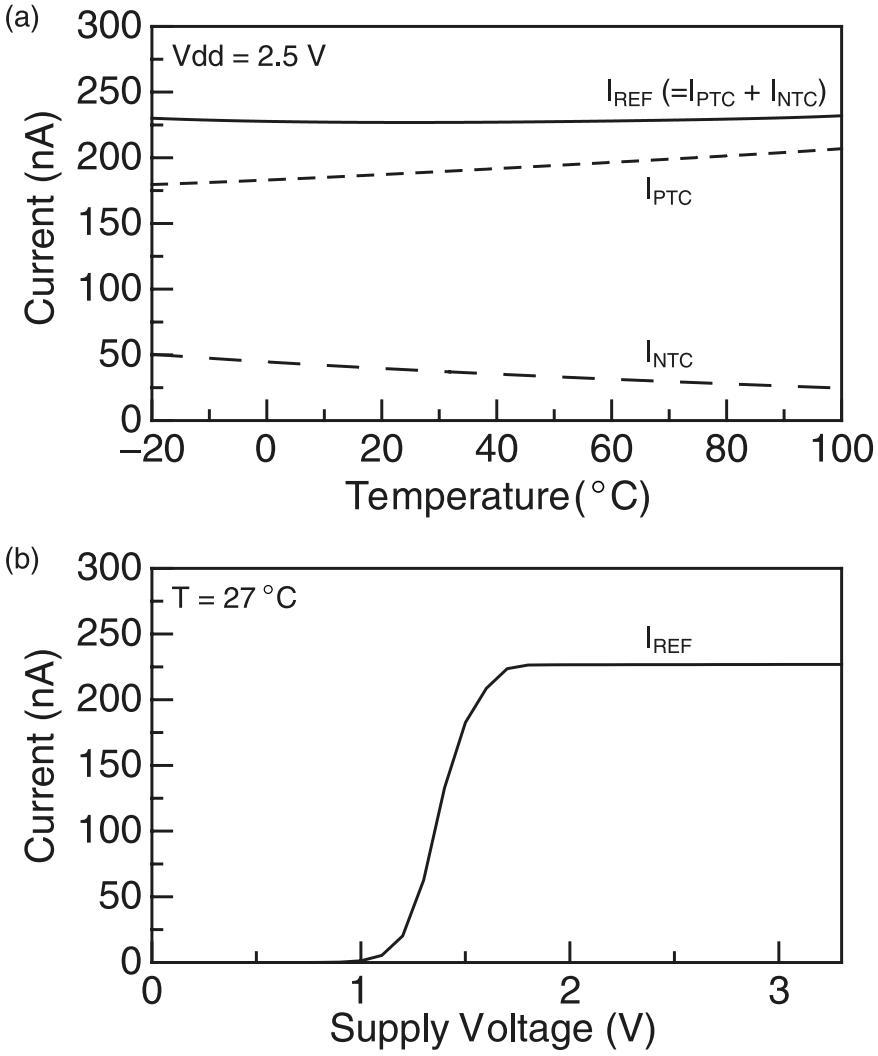

Fig. 2. Simulated reference current I_{REF}: (a) temperature, and (b) power supply voltage dependence.

zero V_{TH0} changes significantly with process corner conditions, but the effect of the threshold voltage change on TC_I of the current is small. Therefore, from the corner analysis, it is clear that almost a constant reference current can be obtained over a wide temperature range.

Although the reference current circuit we proposed can generate a current with little temperature dependence, the absolute value will change according to the process conditions. Therefore, the circuit cannot be used as an ordinary reference circuit. However, the circuit can be used as a bias current generator to compensate for temperature variation in ultralow-power analog circuit systems consisting of an operational amplifier, a comparator, and so on. In addition, in ultralow-power smart sensor LSI applications, because the sensing signal that is the "difference" from the reference current is the most important, the circuit can also be used to extract and process signals from sensor devices.

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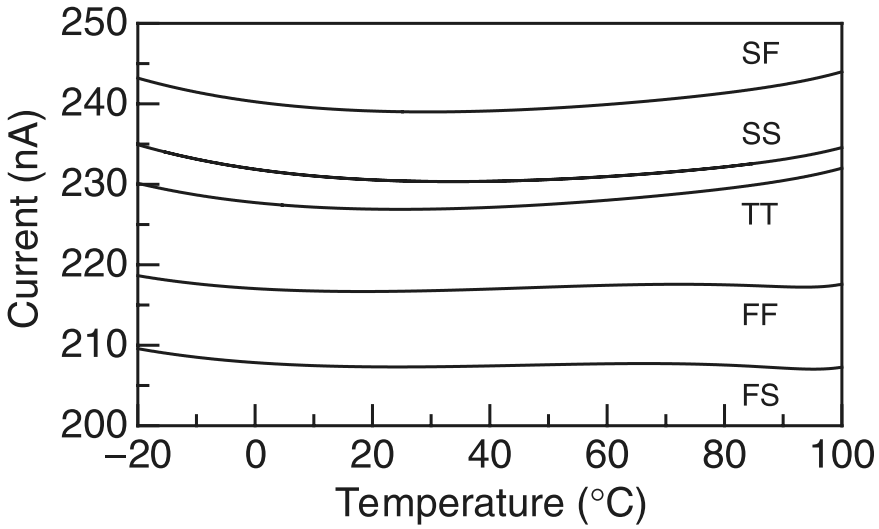

Fig. 3. Simulated temperature characteristics of reference current I_{REF}, assuming five different process corner variations. (SF: slow-fast. SS: slow-slow. TT: typical-typical. FF: fast-fast. FS: fast-slow.)

4 Conclusion

An ultralow power current reference circuit with little temperature dependence was proposed for the power-aware subthreshold LSIs. The circuit consists of a PTC subcircuit, a NTC subcircuit, and a current adder subcircuit. The circuit is useful as a reference current circuit for a micropower LSI applications. A SPICE simulation demonstrated that the reference current was 230 nA, and the variation can be kept very small within ±1.3% in a temperature range of −20 to 100°C, and that the circuit shows a temperature-compensated characteristics with process variation. Standard CMOS technology can be used without a resistor.

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