LETTER *Special Section on Nonlinear Theory and Its Applications*

A CMOS Reaction-Diffusion Circuit Based on Cellular-Automaton Processing Emulating the Belousov-Zhabotinsky Reaction

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SUMMARY   The Belousov-Zhabotinsky (BZ) reaction provides us important clues in controlling 2D phase-lagged stable synchronous patterns in an excitable medium. Because of the difficulty in computing reaction-diffusion systems in large systems using conventional digital processors, we here propose a cellular-automaton (CA) circuit that emulates the BZ reaction. In the circuit, a two-dimensional array of parallel processing cells is responsible for fast emulation, and its operation rate is independent of the system size. The operations of the proposed CA circuit were demonstrated by using a simulation program with integrated circuit emphasis (SPICE).
key words: *reaction-diffusion system, reaction-diffusion chip, cellular automaton, Belousov-Zhabotinsky reaction*

1. Introduction

Controlling 2D phase-lagged stable synchronous patterns called modelock or spiral waves in reaction-diffusion (RD) systems has been highlighted in the field of nonlinear problem [1]. Typically, modelock is a negative factor in artificial systems because of the difficulty in controlling and thus predicting its dynamic behavior. It hampers the desired in-phase synchronization of oscillator arrays, e.g., generating an irregular heartbeat or unpredictable skews in a 2D array of voltage-controlled oscillators for VLSI clocking.

   The Belousov-Zhabotinsky (BZ) reaction, which is a periodic oxidation-reduction phenomenon among liquid-state reagents and is a typical example of RD systems, produces a variety of rhythms and orders in the form of propagating chemical waves [1], [2]. It gives us important clues in controlling modelock phenomena and in revealing the relation between chemical reactions and vital phenomena in nature. A numerical simulation is useful for supporting theoretical research with respect to controlling modelock, however, conventional digital processors are not suitable for computing large-scale RD systems (including the BZ reaction). Custom hardware is thus required for emulating them. In this report, we describe an analog-digital hybrid circuit that

emulates a simplified BZ reaction model. In the circuit, we used a cellular-automaton (CA) architecture to compute the BZ model, aiming at fast emulation independent of the system size.

2. The BZ Reaction Model

Gerhardt et al. proposed a simplified model of the BZ reaction that uses the CA method [3]. The BZ reaction models are mostly described using continuous system variables, but they introduced discrete system variables and discrete time into the CA. In the model, a cell corresponds to a point in the BZ reaction space; e.g., a 2D BZ reaction is imitated by arranging the cells on a grid. Two types of system variables that represent the concentration of $HBrO_2$ and Fe^{3+} ions, U_i and V_i, respectively, were used in the model. The variable U_i takes a binary value, while V_i takes multiple values as $n\,dv$, $(dv = 1/N,\, n = 0, 1, \cdots, N-1)$.

   In the model, three types of reaction states are defined at each cell; i.e., inactive, active, and refractory states. The reaction state of a cell represents the process of the BZ reaction at a point in the reaction-diffusion space. The inactive, active, and refractory states represent a depletion in the Br^- ion, an auto-catalytic increase in the $HBrO_2$ ion (oxidation of the catalyzer), and a depletion in the Br^- ion (reduction of the catalyzer), respectively. Figure 1 shows a circulative state-diagram of a single cell. The reaction states are discriminated by the values of U_i and V_i and are represented by gray boxes in Fig. 1(a). A cell

(a) Discrete BZ model   (b) Sample operation
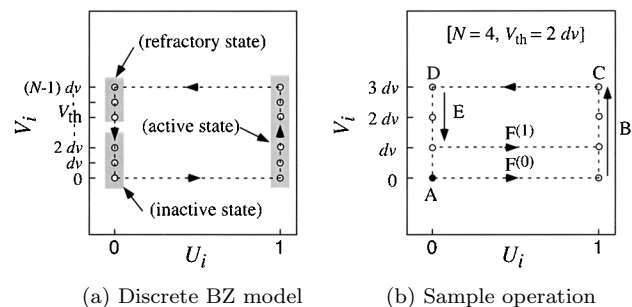
Fig. 1   State diagram of single cell.

can be activated ($U_i = 0 \rightarrow 1$) only when $U_i = 0$ and $0 \leq V_i < V_{\mathrm{th}}$ by collective activations in its neighboring cells [as transition $\mathrm{F}^{(0)}$ or $\mathrm{F}^{(1)}$ in Fig. 1(b)]. During a refractory state ($U_i = 0$ and $V_{\mathrm{th}} \leq V_i \leq (N-1)dv$), the cell cannot be activated by its neighboring cells. Once the cell is activated, the value of V_i is increased as the discrete time step increases [B in Fig. 1(b)]. When the value of V_i reaches its maximum value $(N-1)dv$ [C in Fig. 1(b)], the cell is deactivated and the value of V_i is decreased as the time step increases [D to A in Fig. 1(b)].

3. The CA Circuit for the BZ Model

A CMOS cell circuit, which we denote as a *reaction cell*, is designed to implement the CA model of the BZ reaction. Each reaction cell is arranged on a 2D hexagonal grid and is connected with adjacent cells through *coupling devices*. The coupling device is used to transmit a cell's state to its neighboring cells. To ensure computational accuracy, digital circuits are used for storing a cell's states (values of U_i and V_i). Analog circuits are used for designing a compact cell circuit and for determining the subsequent cell's states.

The cell circuit consists of a digital memory circuit and a transition-decision (TD) circuit. The value of variable U_i is stored in the TD circuit as a binary value, while the value of variable V_i is stored in a conventional N-bit up-down (UD) shift register (Fig. 2) as

$$s_i^{(n)} = \begin{cases} \text{logical ``1,''} & (V_i \geq n\ dv) \\ \text{logical ``0,''} & (V_i < n\ dv) \end{cases},$$

where $n = 1, 2, \ldots N$. The up- or down-operation of the shift register is determined using the value of U_i. When U_i is set at logical "1" (or "0"), the circuit operates as an up (or down) counter, which results in the value of V_i increasing (or decreasing) with the clocks (CLK).

Figure 3(a) shows the part of the TD circuit that compares the cell's states ($s_i^{(1)}$ and $s_i^{(2)}$) with those of its adjacent cells (U_i^1 to U_i^6) using analog operations.
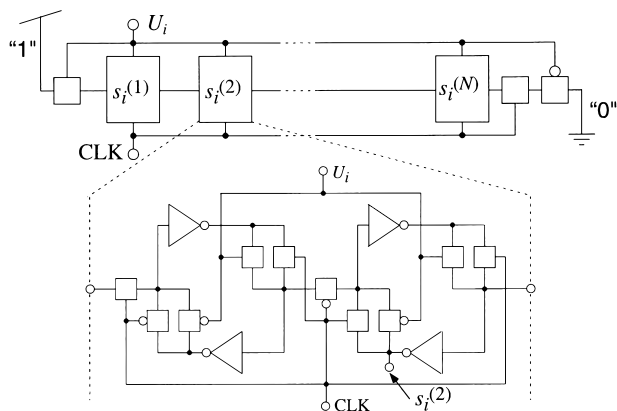
The circuit consists of a νMOS differential amplifier acting as a multi-input (and thus a variable-threshold) comparator. Each circuit has six coupling devices consisting of the floating-gate capacitors of the νMOS transistors and accepts six adjacent inputs (U_i^1 to U_i^6) via the capacitors. Using νMOS transistors make the cell circuit very compact compared with ordinary logic circuits that provide the same functions [4]. The output of the comparator of the i-th cell (VOUT_i) is found using

$$\mathrm{VOUT}_i = \Theta\Big(M_i + \mathrm{VM} - (s_i^{(1)} + s_i^{(2)} + 0.5)\Big),$$

where $\Theta(\cdot)$ represents the step function, M_i the number of active cells around the i-th cell, VM the logical input that determines the excitatory or oscillatory mode, and $s_i^{(1),(2)}$ the output of the i-th shift register. The output becomes logical "1" when $M_i \geq NV_i + 1 - \mathrm{VM}$.

The output of the comparator is connected with the other part of the TD circuit; i.e., a cell state memory [Fig. 3(b)]. It consists of a latch and additional control circuits. The latch stores a cell state U_i according to the state-diagram of the BZ model. We implement the operation of the state-diagram shown in Fig. 1(b) into the CA circuit. The parameter of the cell transition and the refractory threshold V_{th} is controlled by voltage input VM in the comparator and voltage input VT that is connected to terminal $s_i^{(1)}$ or $s_i^{(2)}$ in the UD shift register within the same (i-th) cell.

The latch circuit consists of two inverters (I1 and I2) and two transfer gates (T2 and T4). When the RESET or $s_i^{(N)}$ terminal is set to logical "1," the cell state U_i becomes logical "0" because transfer gate T3 is turned on. The latch circuit receives the output of the comparator (VOUT_i) through transfer gate T1. The gate T1 is turned on (the latch is ready to store the value of VOUT_i) when the cell is active ($U_i = $ logical "1") or $s_i^{(N)} = $ logical "1" or VT = logical "1."

Suppose that the cell state is set at (U_i, V_i) = ("0," "0") at $t = 0$ [A in Fig. 1(b)]. When VM is set at logical "0" (excitatory mode), the cell state does not change with the clocks as long as $M_i = 0$ because VOUT_i is always logical "0." When $M_i > 0$, U_i becomes logical "1" [transition $F^{(0)}$ in Fig. 1(b)], and the value of V_i is increased by the up counter [B in Fig. 1(b)] because U_i is set to "1." When V_i reaches its maximum value, $s_i^{(N)}$
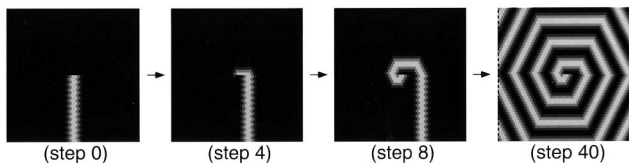

Fig. 2　Up-down shift-register circuit.
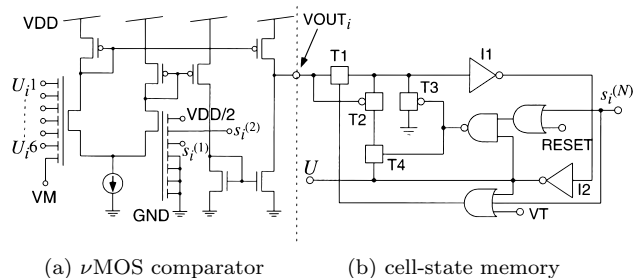
(a) νMOS comparator　　(b) cell-state memory

Fig. 3　Transition-decision circuit.

Table 1 Transition rules for excitatory and oscillatory operation-modes with $N = 4$.

V_i	VM ="0" (excitatory mode)		VM ="1" (oscillatory mode)	
	VT $= s_i^{(1)}$	VT $= s_i^{(2)}$	VT $= s_i^{(1)}$	VT $= s_i^{(2)}$
3 dv	x	x	x	x
2 dv	x	x	x	x
dv	x	2	x	1
0	1	1	0	0

**Fig. 4** Excitatory modelock operations of RD chip.

becomes logical "1" [C in Fig. 1(b)] and the value of U_i is set to logical "0" [D in Fig. 1(b)] by T3. Then, V_i is decreased by the down counter [E in Fig. 1(b)] because U_i is set to logical "0." If $M_i = 0$ during the down-count operation, the cell state (U_i and V_i) is settled at ("0" and "0"). During the down-count operation, U_i becomes "1" again when $M_i \geq NV_i + 1$ and VT is set at logical "1." This transition is regulated by the values of V_i because VT is connected to the terminal $s_i^{(1)}$ or $s_i^{(2)}$. If VT is connected to terminal $s_i^{(2)}$ (or $s_i^{(1)}$), the transition $F^{(1)}$ (or $F^{(0)}$) in Fig. 1(b) can occur when $M_i \geq 2$ (or 1).

On the other hand, if VM is set at logical "1" (oscillatory mode), the cell state is not settled at (U_i, V_i) = ("0," "0") because the output VOUT$_i$ becomes logical "1" when $V_i = 0$. The subsequent operation is the same as the excitatory mode. Table 1 summarizes when the cell transition occurs with respect to the parameters VM and VT. The item values (0, 1, 2) indicate the number of active adjacent cells (M_i) required for the cell transition. The item "x" represents that the transition does not occur with any values of M_i.

To validate the operation of our proposed RD chip, we designed a circuit consisting of 50 by 50 cells and tested its operation using SPICE simulations, assuming a 0.6-μm double-poly CMOS process.

4. Simulation Results

Figure 4 shows an example operation of the CA circuit in excitatory mode ($N = 3$, VM = logical "0," VT was connected to $s_i^{(1)}$). Initial values were set by transmitting binary sequences serially to the digital memory circuits and TD circuits through row-column selectors. Each snapshot was constructed from the serial data representing the cell states by stopping system clocks at steps 0, 4, 8, and 40. Each cell state was represented in grayscale ($V_i = 0$: black, $V_i = (N - 1)dv$: white). In the circuit's initial state, cells adjacent to inactive
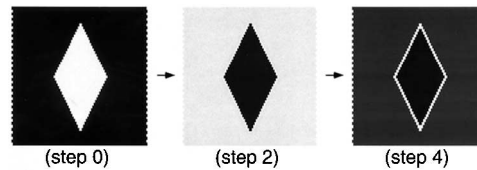
Fig. 5 Oscillatory operations of RD chip.

cells were in a refractory period (step 0 in Fig. 4). The inactive cells adjacent to the white bar in Fig. 4 were suppressed by adjacent cells in the refractory period (cells in the white bar). The inactive cells then entered an active, inactive, or refractory period, depending on the degree of the refractory condition. When the inactive cells were in an active or inactive period, the tip of the bar rotated inward (step 4 to 8 in Fig. 4), resulting in the generation of the modelock (spiral patterns) typically observed in the BZ reaction (step 40 in Fig. 4). A hexagonal distortion of the propagating waves was generated by interactions between adjacent cells.

Figure 5 shows another example-operation of the CA circuit in oscillatory mode ($N = 4$, VM = logical "1," VT was connected to $s_i^{(2)}$). The diamond pattern was given to the circuit as an initial state (step 0). The initial pattern became inverted after two iterations (step 2); the edges of the initial pattern were then extracted after two more iterations (step 4), which represented the same results as the famous demonstration (edge detection) of the BZ reaction [1].

5. Conclusion

We developed a reaction-diffusion (RD) chip based on cellular-automaton processing that emulates the Belousov-Zhabotinsky (BZ) reaction, aiming at developing a custom processor that can serve as a useful tool in exploring large-scale nonlinear systems.

The SPICE simulation showed that the proposed chip can produce typical spatiotemporal patterns observed in the BZ reactions. These results indicate that the proposed RD chip can be easily integrated into existing digital systems and can be used to clarify RD systems, which can be used to develop other novel applications.

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