SILICON IMPLEMENTATION OF A CHEMICAL REACTION–DIFFUSION PROCESSOR FOR COMPUTATION OF VORONOI DIAGRAM

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Reaction–diffusion (RD) chemical systems are known to realize sensible computation when both data and results of the computation are encoded in concentration profiles of chemical species; the computation is implemented via spreading and interaction of either diffusive or phase waves, while a silicon RD chip is an electronic analog of the chemical RD systems where the concentration profiles of chemicals are represented by voltage distributions on the chip's surface. In this paper, we present a prototype RD chip implementing a chemical RD processor for a well-known NP-complete problem of computational geometry — computation of a Voronoi diagram. We offer experimental results for fabricated RD chips and compare the accuracy of information processing in silicon analogs of RD processors and their experimental "wetware" prototypes.

Keywords: Reaction–diffusion system; reaction–diffusion chip; nonstandard computing; cellular automata; Voronoi diagram.

1. Introduction

A reaction–diffusion (RD) processor is a real chemical medium, typically a thin-layer solution, gel or film, which transforms data to results in a predictable, sensible and pre-programmable way. In RD processors data are represented by perturbances of medium's characteristics, e.g. inhomogeneous concentration profile of one reagent. Excitation waves or diffusive waves of reagents travel from the perturbances, interact with each other, and produce either stationary, precipitate concentration profile, or dynamic, oscillatory field, structures. The final state of the medium's spatial dynamics represent a result of the RD computation [Adamatzky, 2001]. Recently experimental prototypes of RD processors were applied to solve a wide range of computational problems, including image processing [Kuhnert, 1989; Rambidi, 1998, 2002; Adamatzky *et al.*, 2002], path planning [Steinbock, 1995; Agladze, 1997; Adamatzky & De Lacy Costello, 2003], logical computation [Tóth & Showalter, 1995; Adamatzky & De Lacy Costello, 2002a; Motoike & Adamatzky, 2005] and robot navigation [Adamatzky *et al.*, 2004b].

Semiconductor RD computing LSIs (chips) implementing RD dynamics have been proposed in the literature. These chips were mostly designed by digital, analog, or mixed-signal complementally-metal-oxide-semiconductor (CMOS) circuits of cellular neural networks (CNNs) or cellular automata (CA). Electrical cell circuits were designed to implement several CA and CNN models of RD systems [Adamatzky *et al.*, 2004a; Asai *et al.*, 2002; Bonaiuto *et al.*, 2001; Matsubara *et al.*, 2004; Rekeczky *et al.*, 2003; Shi & Luo, 2004], as well as fundamental reaction–diffusion equations [Asai *et al.*, 2004; Asai *et al.*, 2005; Daikoku *et al.*, 2002; Karahaliloglu & Balkir, 2004; Serrano-Gotarredona & Linares-Barranco, 2003]. Each cell is arranged on a 2D square or hexagonal grid and is connected with adjacent cells through coupling devices that transmit a cell's state to its neighboring cells, as in conventional CAs. For instance, an analog-digital hybrid RD chip [Asai *et al.*, 2002] was designed for emulating a conventional CA model for Belousov–Zhabotinsky (BZ) reactions [Gerhardt *et al.*, 1990]. A full-digital RD processor [Matsubara *et al.*, 2004] was also designed on the basis of a multiple-valued CA model, called *excitable lattices* [Adamatzky, 2001]. An analog cell circuit was also designed to be equivalent to spatial-discrete Turing RD systems [Daikoku *et al.*, 2002]. A full-analog RD chip that emulates BZ reactions has also been designed and fabricated [Asai *et al.*, 2005]. Furthermore, blue-prints of non-CMOS RD chips have been designed; i.e. a RD device based on minority-carrier transport in semiconductor devices [Asai *et al.*, 2004] and a single-electron RD device [Oya *et al.*, 2005].

To compare the accuracy of information processing in silicon analogs of RD processors and their experimental "wetware" prototypes we selected a well-known NP-complete problem of computational geometry — computation of a Voronoi diagram (VD).

The paper is structured as follows. Section 2 provides a background of the VD problem. Designs and operational characteristics of laboratory chemical processor for VD computation are outlined in Sec. 3. In Sec. 4 we make a logical transition from Euclidean VDs, approximated in chemical processors, to discrete VDs, calculated in RD chips with the help of cellular automaton models. Structure and electronic implementation of silicon RD processor are discussed in Sec. 5. Section 6 discusses the accuracy of information processing in silicon analogs of RD processors and their experimental "wetware" prototypes.

2. Voronoi Diagram

Given a nonempty finite set $\mathbf{P}$ of planar points, a planar Voronoi diagram (VD) of the set $\mathbf{P}$ is a partition of the plane into such regions, that for any element of $\mathbf{P}$, a region corresponding to a unique point p contains all those points of the plane that are closer to p than to any other node of $\mathbf{P}$. A unique region

$$\text{vor}(p) = \{z \in \mathbf{R}^2 : d(p, z) < d(p, m) \\ \forall\, m \in \mathbf{R}^2\, m \neq z\} \tag{1}$$

assigned to point p is called a Voronoi cell. A boundary of the Voronoi cell of a point p is built of segments of bisectors separating the point p and its geographically closest neighbors from $\mathbf{P}$. A union of all boundaries of the Voronoi cells comprises the VD (Fig. 1):

$$VD(P) = \bigcup_{p \in \mathbf{P}} \partial\, \text{vor}(p).$$

A key feature of VD construction is a partition of two- or three-dimensional space on a sphere of influences generated from a given set of objects, points or arbitrary geometrical shapes. Therefore, VDs are
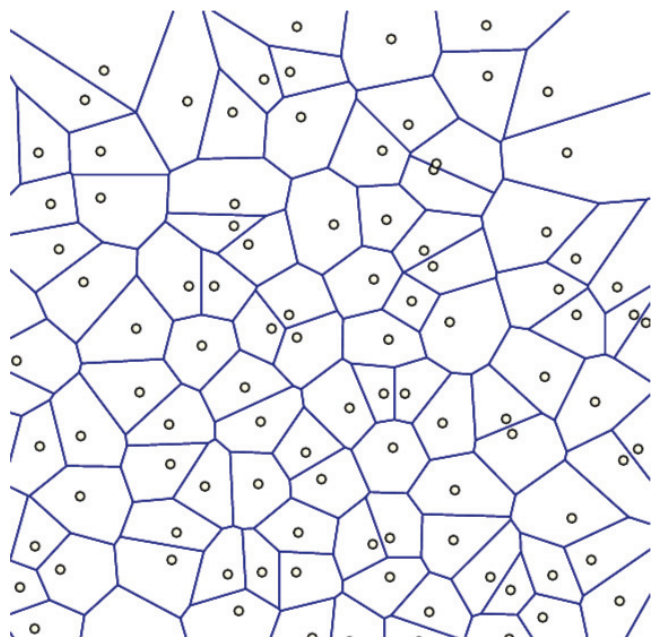

Fig. 1. Voronoi diagrams of planar points computed in GeoWin [Bartuschka *et al.*, 1998–2000].

widely applied in data analysis, like identificaiton of star and galazy clusters [Pasztor, 1994], modeling gravitational influence [Drysdale, 1993], cell and tissue growth [Honda & Eguchi, 1980; Blackburn & Dunckley, 1996], ecological competition models [Barlow, 1974], crystal growth [Hargittai, 1986], market analyses [Okabe *et al.*, 2000], molecular modeling [Pontius *et al.*, 1996], animal skin pigmentation [Walter *et al.*, 1998; Meinhardt, 1995], geographical modeling of surfaces [Bray *et al.*, 1976]. Many computer science applications include pattern recognition (via computation of a skeleton [Adamatzky *et al.*, 2002]), path planning in the presence of obstacles [Earnshaw, 1988], and computer graphics or computer generated images [Deussen *et al.*, 2000]. The Voronoi tessellation is also extensively used in the field of computational geometry where it is applied to solve variations on the nearest neighbor problem [Graham & Yao, 1990; Preparata & Shamos, 1985].

The RD algorithm (CA model) for the computation of a VD was first constructed in [Adamatzky, 1994, 1996]. Experimental prototypes of chemical RD processors were designed in [Tolmachev & Adamatzky, 1996; De Lacy Costello, 2003; De Lacy Costello & Adamatzky, 2003]. The lower boundary of VD computation (of a d-dimensional set of n points) is $\Theta(n)$ and the worst-case complexity is $\Theta(n^{\lceil d/2 \rceil})$ [Preparata & Shamos, 1985]. CA and RD algorithms exploit natural parallelism of the problem, namely distance between neighboring points is represented by time of wave-front traveling in the space, therefore time complexity of VD computation in RD medium is determined by a maximum distance between two geographically neighboring points of given set, which in turn is limited by a diameter D of the given planar set. That is, the worst-case complexity of RD computation of VD is $\Theta(D)$, independent dimension and number of points. Assuming, we can pack given set-preserving topological relationships between its element, the lower boundary will be $\Theta(\sqrt[d]{n})$, in the d-dimensional case.

3. Chemical Implementation of Voronoi Diagram

In experimental prototypes of RD processors for computation of VD, an initial set of data objects (points, segments or shapes) is represented by a concentration profile of one reagent, a planar substrate contains another reagent. The reagent, representing the data objects diffuses to form a colored phase in a reaction with the substrate-reagent. At sites where two diffusion wave fronts meet, no colored phase is formed and the substrate retains its uncolored state. These uncolored loci of the computation space represent edges of required VD. To compare accuracy of results produced by silicon RD chips with those developed in experimental chemical RD processors, we employed three variations of chemical processors, originally described in [De Lacy Costello *et al.*, 2004a, 2004b].

3.1. *Semi-stable copper processor*

Agarose gel (2% by weight, Sigma-Aldrich) with 0.09 M potassium ferricyanide $K_3[Fe(CN)_6]$ (Merk) was prepared and poured into Petri dishes (gel layer 6 mm), and allowed to cool. A 2.93 M solution of $CuCl_2$ was also prepared. The gel surface was marked with a glass pipette and 5 mm of the outer electrolyte was poured onto the gel. VDs are formed in a controlled manner as the centers of the cells are where the gel surface has been marked. Without marking a homogeneous precipitate would have resulted [Fig. 2(a)].

3.2. *Palladium processor*

A gel of agar (1.5% by weight, agar select Sigma–Aldrich Company Ltd. Poole, Dorset, BH12 4XA) containing palladium chloride (Palladium (II) chloride 99%, Sigma Aldrich Company Ltd.) in the range 0.2%–0.9% by weight (0.011–0.051 M) was prepared by mixing the solids in warm deionised water. The mixture was transferred to Petri dishes. The unreacted gel processors were then kept for 30 min. A saturated solution (at 20°C) of potassium iodide (ACS reagent grade, Aldrich Chemical Co.) was used as the outer electrolyte for the reactions. Shapes (to be separated by VD) were made from filter paper and soaked with outer electrolyte before being placed on the gel surface [Fig. 2(b)].

3.3. *Prussian blue processor*

The second type of reaction–diffusion processors employs the ferric ion/ferrocyanide couple where the primary product formed is ferric ferrocyanide (prussian blue, $Fe_4(Fe(CN)_6)_3$). Potassium ferrocyanide ($K_4Fe(CN)_6 \cdot 3H_2O$) 2.5 mg/ml (5.91 mM) ((99+%) BDH Chemicals Ltd., Poole, Dorset) was mixed with a 1.5% gel of agar (Agar, select, Sigma chemical company). The mixture was heated with
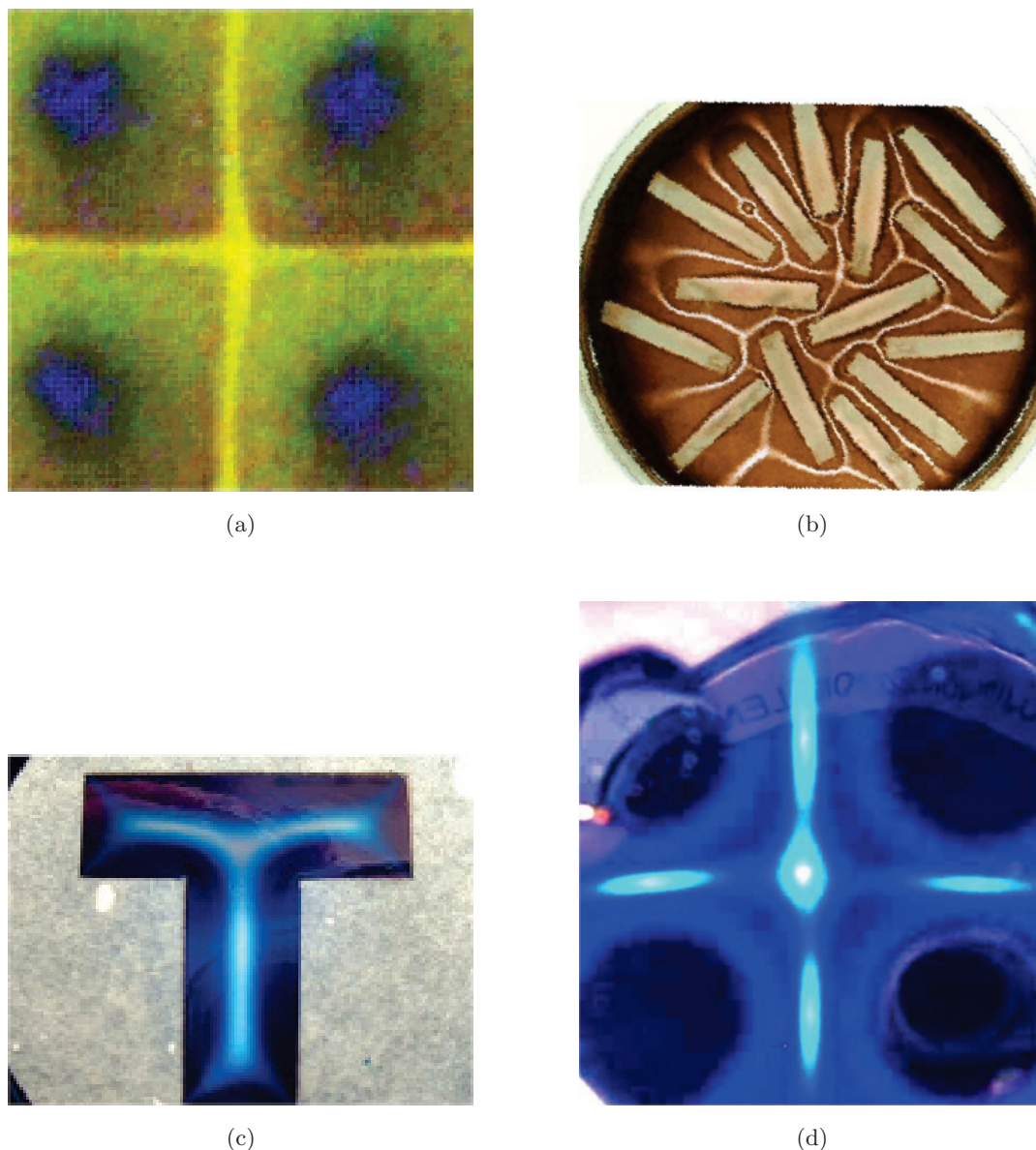
(a)

(b)

(c)

(d)

Fig. 2.   Voronoi diagrams of (a) four points computed in unstable copper processor, (b) rectangles computed in palladium processor, (c) T-shape computed in Prussian blue processor, (d) four points computed in stable Prussian blue processor.

a naked flame until boiling and then removed from the heat and decanted into Petri dishes (5 ml per plate). A Ferric ion solution was used as the outer electrolyte (300 mg/ml, 0.74 M, Iron (III) nitrate nonahydrate, but any highly pure soluble ferric ion source will suffice, 99.99+%, Aldrich Chemical Company). The processor was used to calculate the internal Voronoi diagram, or skeleton, of a planar T-shape. The T-contour was cut out from off from filter paper and saturated with the outer electrolyte before being placed on the gel [Fig. 2(c)]. Alternatively, drops of the outer electrolyte were placed onto the gel surface [Fig. 2(d)].

4.   Cellular Automaton Computation of Voronoi Diagram

To design a silicon analogue of RD "wetware" processors we must firstly uncover an abstract mechanic of computation in experimental chemical devices, and only then transfer key rules of micro-volume state transitions to electronic schemes of elementary units of RD chips. We will use cellular automata as a device transient between real-life chemistry and silicon chips. A cellular automaton (CA) is a two-dimensional array of finite automata, which updates their states in parallel, in discrete time, and depending on states of their closest neighbors.

Let us consider the following model, RD chemical excitable model $\mathcal{A}_1$. Cells of the automaton take state from interval $[\rho, \alpha]$, where ρ is a minimum refractory value, and α is maximum excitation value; $\rho = -2$ and $\alpha = 5$ in our experiments. Cell x's state transitions are strongly determined by normalized local excitation $\sigma_x^t = \sum_{y \in u_x}(y^t / \sqrt{(|u_x|)})$. Every cell x updates its state at time $t + 1$, depending on its state x^t and state u_x^t of its neighborhood u_x (in experiments we used 15×15 cell neighborhood) as follows:

$$x^{t+1} = \begin{cases} \alpha, & \text{if } x^t = 0 \text{ and } \sigma_x^t \geq \alpha \\ 0, & \text{if } x^t = 0 \text{ and } \sigma_x^t < \alpha \\ x^t + 1, & \text{if } x^t < 0 \\ x^t - 1, & \text{if } x^t > 1 \\ \rho, & \text{if } x^t = 1 \end{cases}$$

This is how "excitation" spreads in computational space, waves of excitation interact and annihilate. To allow the processor to memorize sites of wave collision we added a precipitate state p_x^t of cell x. Concentration p_x^t of precipitate at site x at moment t is calculated as $p_x^{t+1} \sim |\{y \in u_x : y^t = \alpha\}|$.

CA $\mathcal{A}_1$ computation of VD of four points, two segments are shown in Figs. 3(a) and 3(b), and approximation of internal VD, or a skeleton, in Fig. 3(c). The model $\mathcal{A}_1$ represents VD in "unlike phase" with experimental chemical representation of VD: sites of higher concentration of precipitate in configurations of $\mathcal{A}_1$ correspond to sites with lowest precipitate concentration in experimental processors. Comparing diagrams computed by CA $\mathcal{A}_1$ with those developed in RD experimental chemical processors, Fig. 2, we find that there is a remarkable correspondence between density distribution in bisector representation and geometry of bisectors.

Despite being pleasantly naturalistic the model $\mathcal{A}_1$ might be too complicated for LSI implementation. So, we have simplified $\mathcal{A}_1$ to model $\mathcal{A}_2$ by assuming that every cell takes just four states, resting $\circ$, excited $+$, refractory $-$, and precipitate $\#$. A cell in $\mathcal{A}_2$ updates its state as follows:

$$x^{t+1} = \begin{cases} +, & \text{if } x^t = \circ \text{ and } 0 < \eta_x^t \leq 4 \\ \#, & \text{if } ((x^t = \circ \text{ or } x^t = +) \text{ and } \eta_x^t > 4) \\ & \quad \text{or } x^t = \# \\ -, & \text{if } x^t = + \text{ and } \eta_x^t \leq 4 \\ \circ, & \text{otherwise} \end{cases} \quad (1)$$
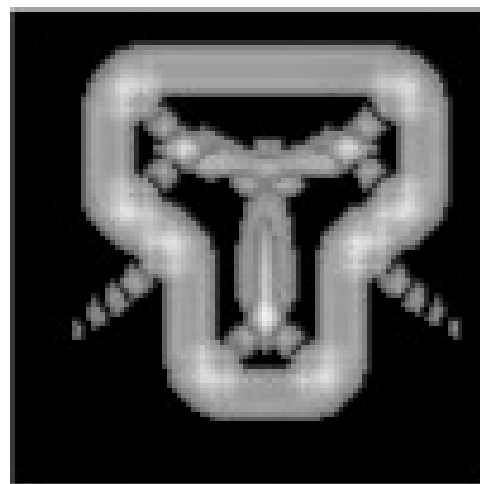
Model $\mathcal{A}_2$ was discussed in detail in [De Lacy Costello *et al.*, 2004], so we do not study it in detail
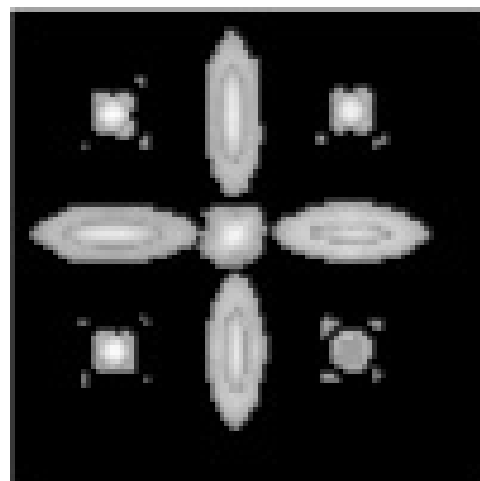
(a)
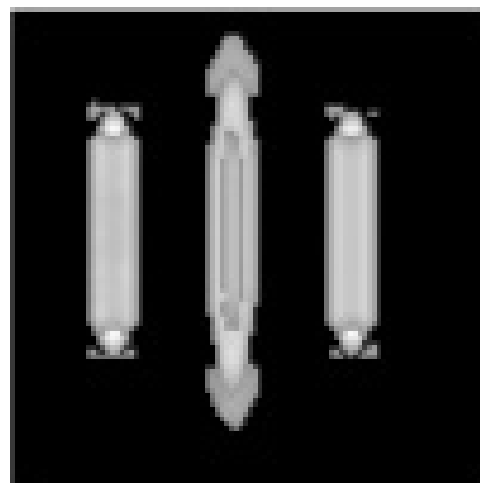
(b)

(c)

Fig. 3. Voronoi diagrams of (a) four points, (b) two line segments, (c) T-shape computed in CA model $\mathcal{A}_1$.

in the present paper, but instead move straight to the silicon implementation.

5. Silicon Implementation of CA VD Model

We designed electrical circuits implementing model $\mathcal{A}_2$, which was previously given by Eq. (1) in the preceding section, for VD computation and skeletonization. Each cell of the CA is implemented on a unit (cell) circuit, which results in the two-dimensional array construction of the cell circuits. To increase the integration density of the cell circuits, each cell circuit has to be designed as compact as possible. Therefore we propose an analog-digital hybrid circuit for the cell.

To store the four types of cell states in model $\mathcal{A}_2$, i.e. resting ∘, excited +, refractory −, and precipitate #, we employ a 2-bit static memory (two D-type flip-flop circuits: D-FFs) for each cell. The cell state is encoded in 2-bit binary values, as shown in Table 1. A cell's state encoded in the memory is updated according to the current state of the cell

and the number of excited cells among its neighboring cells.

The cell transition (1) is represented by a transition table shown in Table 2. In the table, q_1 and q_2 represent the present state of a cell in 2-bit binary values (see Table 1 for translation), s_n is a binary value that becomes logical "1" when the number of surrounding excited cells exceeds n (otherwise s_n is logical "0"), d_1 and d_2 represent the subsequent state of a cell after the transition. If a cell is in its excited state $[(q_1, q_2) = (\text{"1"}, \text{"1"})]$ and the number of excited cells among the neighbors exceeds 4 ($s_4 = \text{"1"}$), the subsequent cell state is set at precipitate $[(d_1, d_2) = (\text{"1"}, \text{"0"})]$. If $(q_1, q_2) = (\text{"1"}, \text{"1"})$ and $s_4 = \text{"0"}$, the subsequent cell state is refractory

Table 1. Translation table of the cell states.

Cell State	q_1	q_2
Resting (∘)	"0"	"0"
Refractory (−)	"0"	"1"
Precipitate (#)	"1"	"0"
Excited (+)	"1"	"1"

Table 2. Translation table of the cell states. "×" represents "no matter".

# of Excited Neighbors		Current State		Subsequent State		Transition
> 0 (s_0)	> 4 (s_4)	q_1	q_2	d_1	d_2	$t \rightarrow t + \Delta t$
×	"1"	"1"	"1"	"1"	"0"	$+ \rightarrow \#$
×	"0"	"1"	"1"	"0"	"1"	$+ \rightarrow -$
×	"1"	"0"	"0"	"1"	"0"	$\circ \rightarrow \#$
"1"	"0"	"0"	"0"	"1"	"1"	$\circ \rightarrow +$

$[(d_1, d_2) = (\text{"0"}, \text{"1"})]$. If the current cell is resting $[(q_1, q_2) = (\text{"0"}, \text{"0"})]$ and $s_4 = \text{"1"}$, the subsequent cell state is precipitate $[(d_1, d_2) = (\text{"1"}, \text{"0"})]$. If $(q_1, q_2) = (\text{"0"}, \text{"0"})]$ and $s_0 = \text{"1"}$, the subsequent cell state is excited $[(d_1, d_2) = (\text{"1"}, \text{"1"})]$. Otherwise, no transition occurs. This indicates that transition occurs only when the current cell state matches the four cases above, i.e. when $d_1 + d_2 =$ logical "1".

We design a logic circuit that determines the subsequent state of a cell. We call the circuit "transition-decision circuit" (TD circuit). From Table 2, we easily obtain

$$d_1 = s_4 q_1 q_2 + s_4 \overline{q}_1 \overline{q}_2 + s_0 \overline{s}_4 \overline{q}_1 \overline{q}_2$$
$$= s_4 q_1 q_2 + \overline{q}_1 \overline{q}_2 (s_0 + s_4),$$
$$d_2 = \overline{s}_4 (q_1 q_2 + s_0 \overline{q}_1 \overline{q}_2).$$
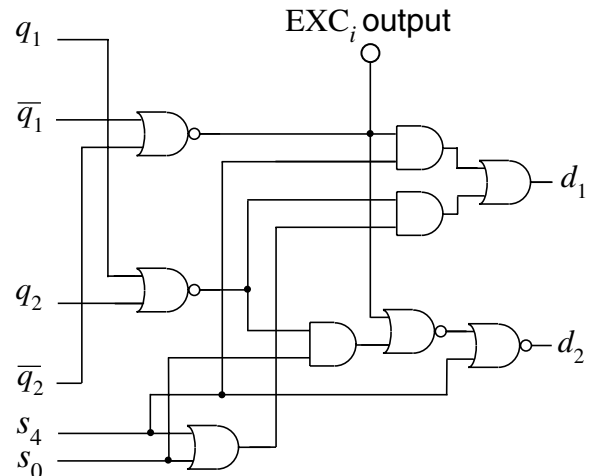

Fig. 4. Transition-decision circuit.

Figure 4 shows a basic construction of the TD circuit that is implemented by conventional logic gates. As described in the previous section, a cell state is changed by the number of its surrounding "excited" cells. In order to give the "excited" information to its neighbors, the TD circuit produces a signal EXC_i where EXC_i becomes logical "1" only when $(q_1, q_2) = ($ "1", "1" $)$ (otherwise, EXC_i is "0").

Here, s_n is a binary value that represents whether the number of surrounding excited cells exceeds n or not. To obtain s_n signals, we must count the number of surrounding excited cells.
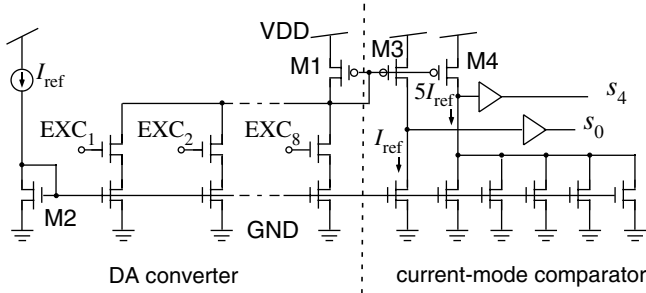

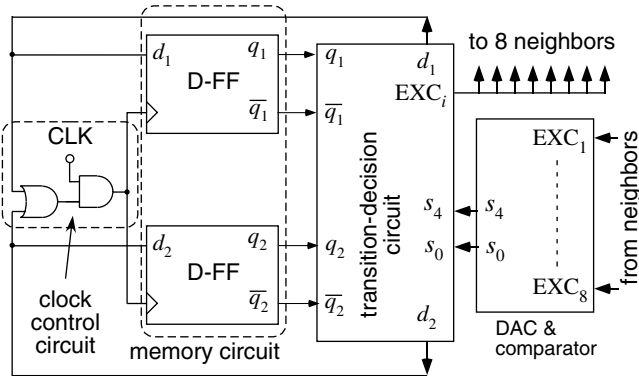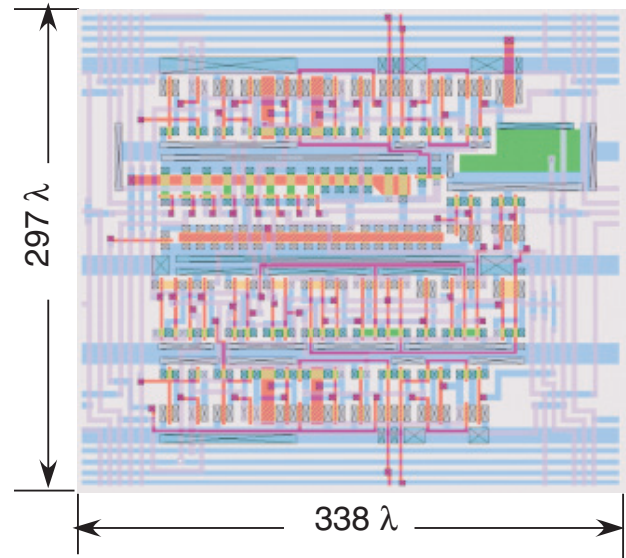Fig. 5. DA converter and current-mode comparator.

Fig. 6. Cell circuit for model $\mathcal{A}_2$.

(MOSIS AMIS 0.5 µm 2-poly3-metal SCMOS)

Fig. 7. Cell layout including a photo detector, TD circuit, DA converter, current-mode comparator, 2-bit memory circuits, and clock control circuit.
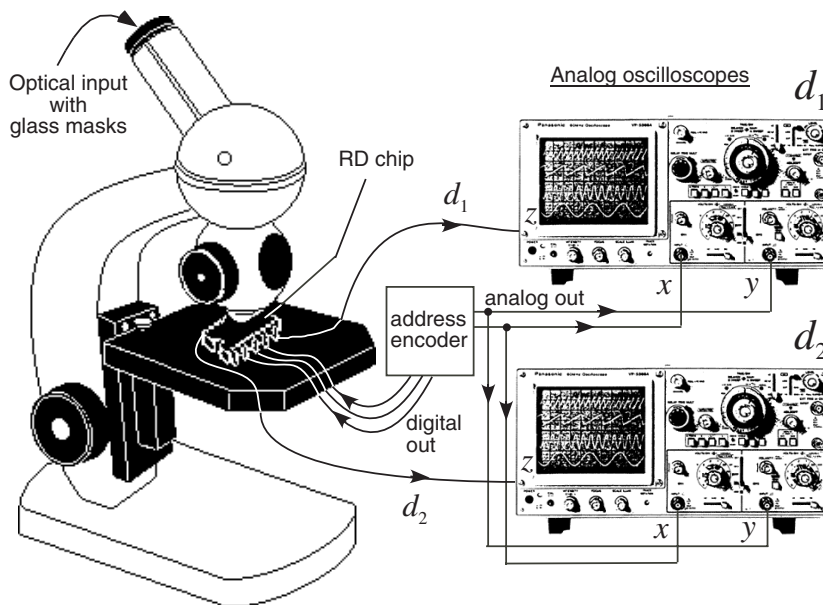

Fig. 8. Experimental setup.

Model $\mathcal{A}_2$ requires both s_0 and s_4 signals because of conditions $\eta_x^t > 0$, $\eta_x^t \leq 4$ and $\eta_x^t > 4$ in Eq. (1). To detect them, we designed a current-mode analog circuit, as shown in Fig. 5. The circuit consists of a conventional DA converter and current-mode comparator. In the circuit, dimensions of all MOS transistors are identical. The DA converter receives EXC_i signals from its eight neighbors (EXC_1, EXC_2, ..., EXC_8). The current M1 is obtained by multiplying I_{ref} by the number $\mathrm{EXC}_i =$ "1" because the current M2 ($= I_{\mathrm{ref}}$) is copied to all nMOS transistors whose source terminal is connected to the ground, and nMOS transistors receiving EXC_is act as current switches. The current M1 is copied to M3 and M4. If the current M3 is

larger than M2 ($= I_{\mathrm{ref}}$), s_0 becomes "1", and if the current M4 is five times larger than M2 ($= 5I_{\mathrm{ref}}$), s_4 becomes "1". This circuit is quite compact as compared with conventional digital counters. Therefore it is useful for large scale integration of RD cell circuits.

The output of the TD circuit (d_1, d_2) are directly connected to the memory circuits (D-FFs). Now assume that the current cell state stored in the D-FFs (q_1, q_2) satisfied one of the conditions listed in Table 2. A clock signal ϕ is given to the D-FFs through a clock control circuit that provides ϕ to the memory circuits only when $d_1 + d_2 =$ "1". Thus, the D-FFs capture input data (d_1, d_2) and update the current state (q_1, q_2) to (d_1, d_2). Figure 6
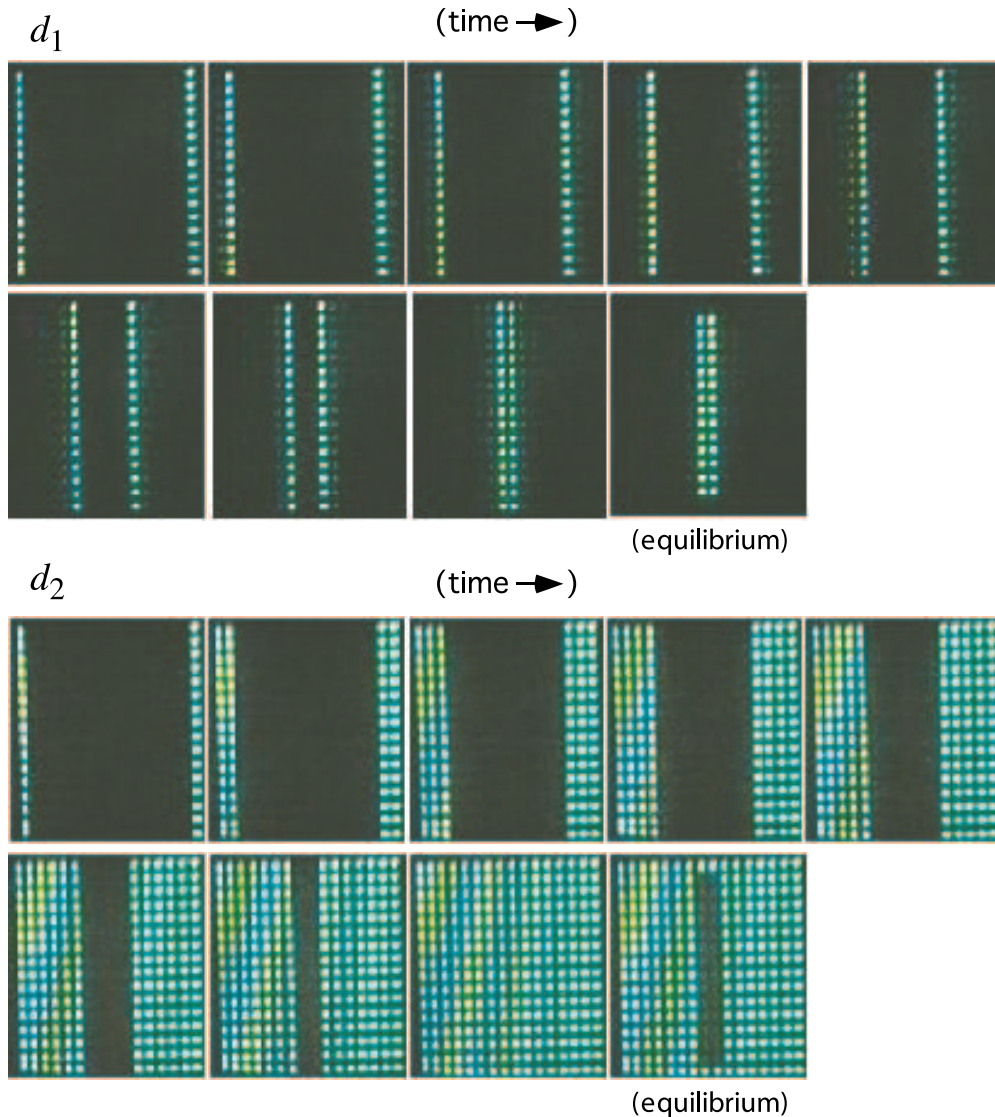

Fig. 9.   Spatiotemporal patterns on the fabricated RD chip (VD operation with two bars).

shows the entire construction of a cell circuit that consists of a TD circuit, DA converter, current-mode comparator, memory circuits and clock control circuit.

We fabricated a prototype CA RD chip that implements 16×16 cells using 0.5-μm double-poly triple-metal n-well CMOS process (MOSIS, Vendor: AMIS). The chip can accept parallel optical inputs, which is very useful for parallel image-processing applications. Figure 7 shows the layout of a cell circuit, including a photo detector (simple pn junction between p-substrate and n-diffusion) and additional switching circuits for reset and readout operations. All circuit areas except for photodetectors were masked by top metal. The resulting cell size was $297\,\lambda \times 338\,\lambda$ ($\lambda = 0.3\,\mu$m).
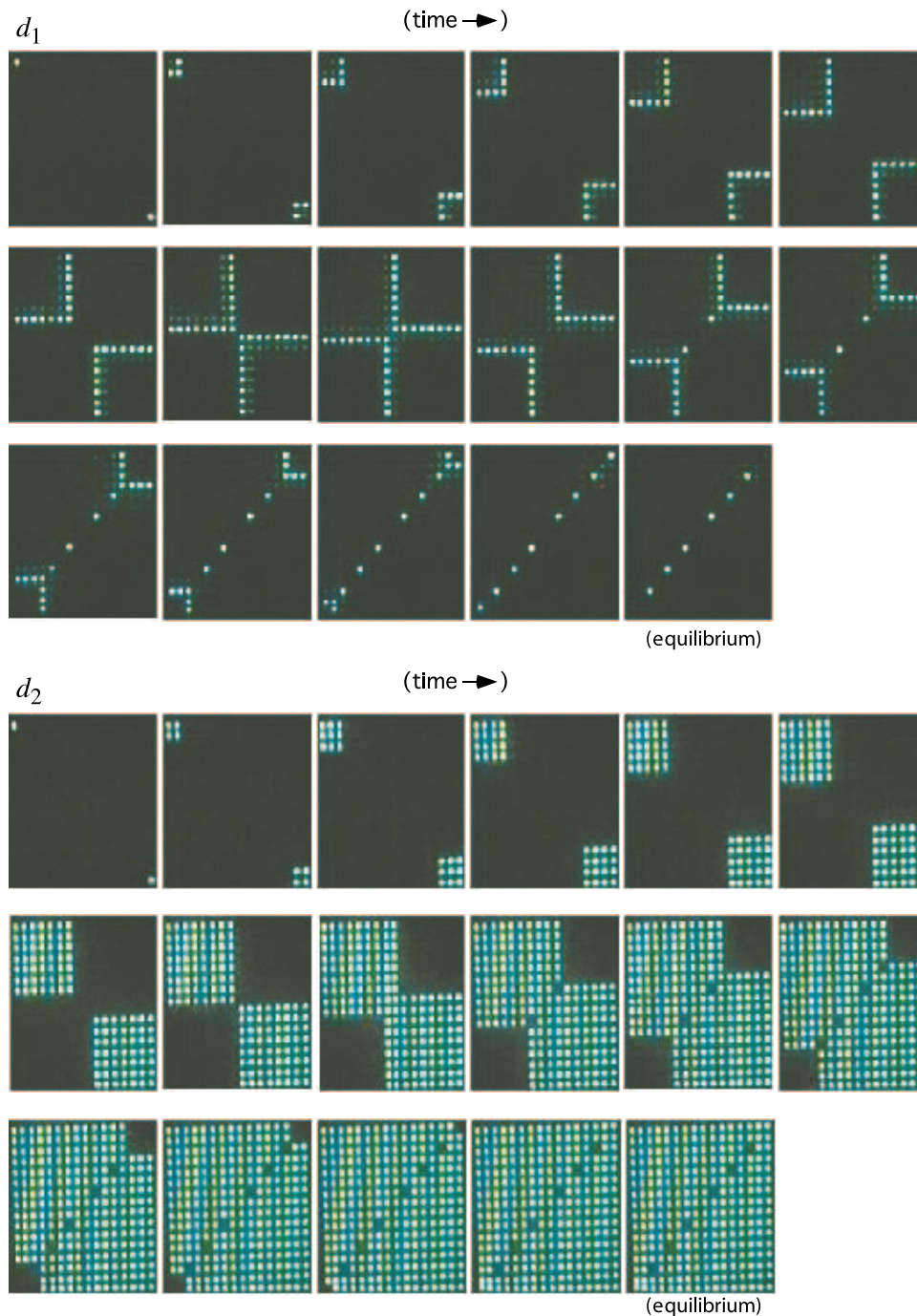

Fig. 10.   Spatiotemporal patterns on the fabricated RD chip (VD operation with two points).

We recorded spatiotemporal patterns of the fabricated RD chip with the following readout circuitry. Figure 8 shows our experimental setup. Initial patterns were given by optical images through a microscope where bright areas were set as "excited" states and dark areas were set as "resting" states. In the fabricated RD chip, each cell circuit was located beneath a wire crossing row- and column-address buses, and was connected to two common-output wires through a transfer gate. This gate connects the cell's output to the common wires when both the row and column buses are active. Thus a cell's outputs (d_1 and d_2) appeared on the common output wires when the cell was selected by activating the corresponding row and column buses simultaneously. We could obtain a binary stream from the common output wires by selecting each cell sequentially. Using a conventional display technique with an external address encoder that produces both analog and digital addressing signals, the binary streams of d_1 and d_2 were reconstructed on analog oscilloscopes operating in x–y Lissajous modes where z [brightness at (x, y)] accepts d_1 or d_2. Therefore, we can observe spatiotemporal patterns of d_1 and d_2 as brightness in the display.

Figure 9 shows the snapshots of the displays we recorded. Each bright spot represents a cell where d_1 or d_2 is logical "1". In the experiment, the supply voltage was set at 5 V, and the system clock was set at low frequency (2.5 Hz) so that "very-slow" spatiotemporal activities could be observed visually (the low frequency was used only for the visualization, and was not the upper limit of the circuit operation). First, we applied bar-shape light to cells on the left and right of the chip. The circuit exhibited the expected results; i.e. two excitable waves of excited cells triggered by the side cells propagated toward the center and precipitated when they collided.

Figure 10 shows other snapshots with different initial conditions. In this experiment, we applied pin-spot lights to two cells at top-left and bottom-right corners of the chip. Two excitable waves were generated by these trigger inputs. When they collided, diagonal cells were precipitated, as expected. These results indicate that the fabricated chip could produce a VD diagram, although the spatial resolution is low in the prototype chip.

Figures 11 and 12 show examples of skeleton operation of a T and "+" shaped images. As initial images, we make a glass mask where "T" and "+" areas are exactly masked. Therefore, cells under the "T" and "+" areas are initially resting and the rest are initially excited. At its equilibrium, skeletons of "T" and "+" were successfully obtained.
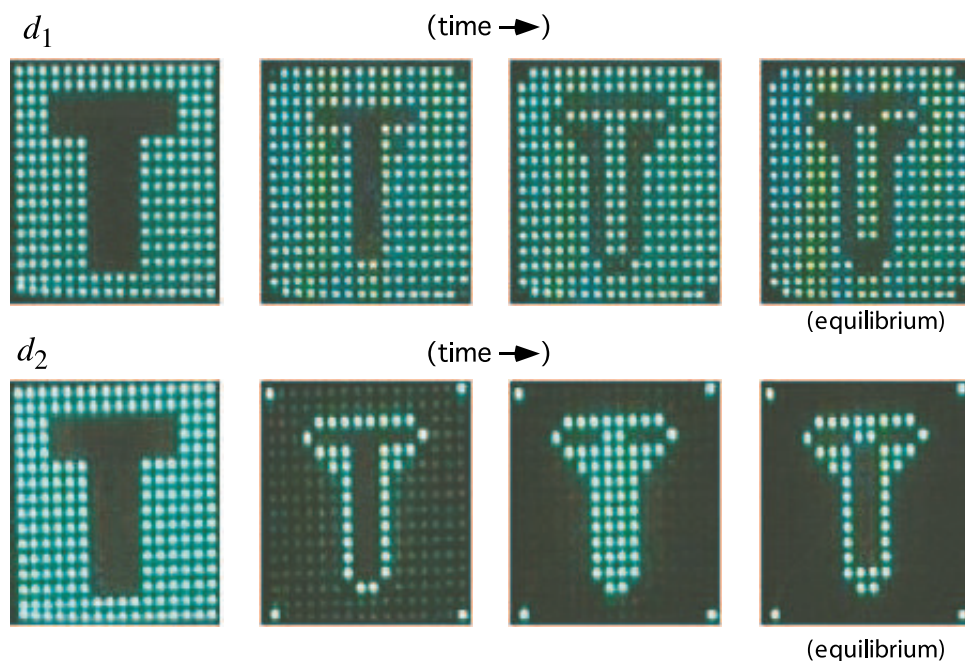

Fig. 11.   Spatiotemporal patterns on the fabricated RD chip (skeleton operation with "T" shape).
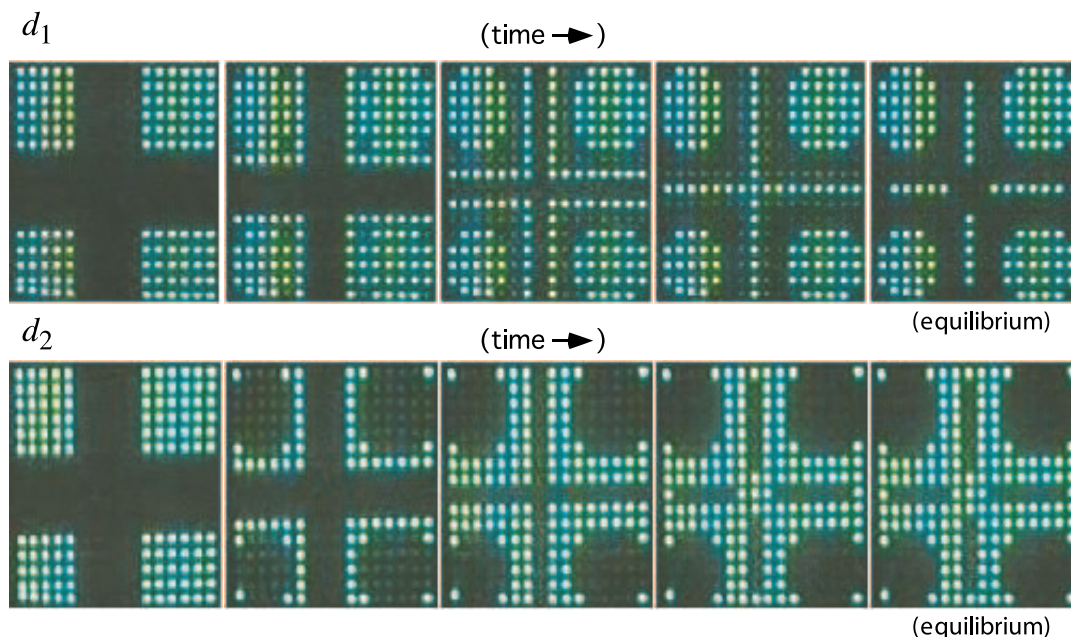
Fig. 12.   Spatiotemporal patterns on the fabricated RD chip (skeleton operation with "+" shape).

6.   Chemicals versus Silicon

We discussed the formation of Voronoi diagrams in spatially extended two-dimensional nonlinear systems: experimental chemical processors, cellular-automaton models and LSI chips. The underlying microscopic processes in these systems are absolutely different, however phenomenology of pattern formation is remarkably similar and thus allowed us to employ interaction of spreading pattern in constructing bisectors of the diagram.

In all systems propagating fronts are initiated at given planar points, in each particular system the fronts propagate with the same speed and thus fronts initiated at two neighboring points collide at sites equidistant from these points. Thus geographically neighboring points "detect" and "interact" with each other by means of spreading patterns. Using biological analogies we can say that the data points expand their "receptive" fields until they encounter "receptive" fields of other data points.

In principle, one could use classical excitable media to subdivide the space into Voronoi cells [Adamatzky & De Lacy Costello, 2002b]. However, excitation waves always annihilate when they collide, and sites of the wave front collision return to original resting state. Thus excitable media based processors do not produce stationary outputs, and special computational techniques would be required to extract the results of the computation. Therefore,

in our studies we used precipitating chemical systems. We included a dedicated precipitate state (a site in precipitate state remains in this state forever) in our cellular-automaton models and their LSI prototypes, and determined that when two or more excitation wave fronts interact (which is detected from local configuration of excited and refractory sites) a precipitate is formed. The approach proved to be efficient, as demonstrated in Secs. 4 and 5, however we were unable to find excitable chemical systems which could produce precipitate during interaction of excitation wave fronts. Therefore, we adapted the algorithm to nonexcitable but precipitating systems: in these systems the precipitate is formed when reagents in the diffusive wave-front interact with reagents in the planar substrate, and thus every data point becomes a source of a growing precipitate domain. The diffusive wave-front causes an influx of substrate reagents along vectors opposite to those of normals of the front. Thus at the sites of collision of two or more diffusive wave-fronts the substrate reagent is exhausted and no precipitate is formed. Bisectors of Voronoi diagram in this case are represented by medium sites without a precipitate.

In semi-stable copper system the inhomogeneties introduced into the gel cause precipitation not to occur at these points. However, as the diffusion front moves through the gel these points expand into empty precipitate free cones. When the

regressing edges of the expanding cones meet the precipitation stops and a VD of the original points marked on the gel is formed. In this case the bisectors are high precipitate regions unlike the stable system.

LSI, chemical and automaton models possess the same degree of complexity. We demonstrated that Voronoi diagram can be constructed in chemical systems with two reagents (which produce one precipitate) and in discrete models with two nonquiescent states and a precipitate state, i.e. elementary processors have finite memory. All prototypes compute Voronoi diagram in time proportional to maximum distance between two geographically neighboring points, i.e. time complexity has boundary $O(\log D)$, where D is a diameter of data planar set, i.e. virtually independent of number of data points. The only disadvantage of the approach is that the linear size of reaction–diffusion processors, computing the diagram, is bounded by D from below, which gives us not too satisfactory boundary of space complexity $o(D)$.

All prototypes discussed in the paper approximate Voronoi diagram sufficiently well for their metrics. Namely, chemical processors approximate Euclidean Voronoi diagram, cellular-automaton model $\mathcal{A}_2$ and LSI chip compute the diagram in metric L_∞ (and thus the resulting patterns are "allowed" to have incomplete bisectors, as discussed in [Adamatzky, 1996]); automaton model $\mathcal{A}_1$ gives us a kind of discrete approximation of the Euclidean diagram.

Obviously, the silicon analogues and CA models can compute VD with much greater speed than their chemical counterparts which can take minutes or hours depending on the system (excitable and unstable systems are faster). Another constraint of practical use of chemical systems is the large size. Currently the minimum point size is limited by a liquid drop size or an introduced inhomogeneity in a gel — therefore cell size is limited to circa $1\,\mathrm{mm}^2$.

7. Summary

In this paper, we discussed the formation of Voronoi diagrams in spatially extended two-dimensional nonlinear systems: experimental chemical processors, cellular-automaton models and LSI chips. We offered experimental results of fabricated RD chip and compared the accuracy of information processing in silicon analogs of RD processors and their experimental "wetware" prototypes. The underlying microscopic processes in these systems are absolutely different, however phenomenology of pattern spreading is remarkably similar and thus allowed us to employ interaction of spreading pattern in constructing bisectors of the diagram.

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