International Journal of Bifurcation and Chaos, Vol. 16, No. 1 (2006) 207–212

A SUBTHRESHOLD ANALOG MOS CIRCUIT FOR LOTKA–VOLTERRA CHAOTIC OSCILLATOR

TETSUYA ASAI*, TAISHI KAMIYA, TETSUYA HIROSE and YOSHIHITO AMEMIYA

Graduate School of Information Science and Technology,
Hokkaido University, Kita 14, Nishi 9,
Sapporo, 060-0814, Japan
**asai@sapiens-ei.eng.hokudai.ac.jp*

Received December 16, 2004; Revised January 11, 2005

We fabricated an analog integrated circuit (IC) that implements the Lotka–Volterra (LV) chaotic oscillator presented by Mimura and Kan-on [1986]. The LV system describes periodic or chaotic behaviors in prey–predator systems in simple mathematical form, and is suitable for analog IC implementation [Asai *et al.*, 2003]. The proposed circuit consists of a small number of metal-oxide-semiconductor field-effect transistors (MOS FETs) operating in their subthreshold region. A new scaling factor of system variables, which was not discussed in [Asai *et al.*, 2003], is also introduced for quantitative studies of designing practical hardware LV systems.

Keywords: Chaotic oscillator; analog integrated circuits; subthreshold MOS circuit; Lotka–Volterra system.

1. Introduction

The design of chaotic oscillators has been the subject of increasing interest during the past few years [Chen & Ueta, 2002; Radwan *et al.*, 2003]. Indeed, analog integrated circuits that implement chaotic oscillatory systems provide us with important clues for exploring and discovering novel forms of information processing. Many designs for chaotic oscillators were introduced starting with the use of a coil in Chua's circuit [Matsumoto *et al.*, 1985] to the use of large blocks such as operational amplifiers [Elwakil & Soliman, 1998a, 1998b]. In both cases, the fabrication area was very large. These designs were also dependent on the use of floating capacitors, high supply voltage and high power dissipation, which are not preferred due to the current demand for portability. In this paper, we propose micropower analog MOS circuits that exhibit chaotic behaviors with very simple circuit construction.

Although there are numerous simple chaotic equations [Sprott, 2000a–2000c; Chen & Ueta, 2002], we have only employed a three-variable Lotka–Volterra (LV) equation. The advantages of the LV system are in its simplicity, absence of multiplication terms with nonlinear transform of system variables [Asai *et al.*, 2003], ease of scaling over a wide range of frequencies, and ease of construction. The proposed circuit is designed based on the use of subthreshold metal-oxide-semiconductor field-effect transistors (MOS FETs) and three grounded capacitors for realizing the LV equation, which is the minimum requirement for the implementation of a chaotic oscillator. This circuit operates on low-supply voltage (2.5 V) and all MOS-FETs operate in their subthreshold region. In this sense, the proposed circuit overcomes the previously mentioned drawbacks and can be used in manufacturing portable devices.

2. Analog MOS Circuits for Lotka–Volterra Model with Two Preys and One Predator

The Lotka–Volterra (LV) model is one of the earliest predator–prey models to be based on sound mathematical principles. It forms the basis of many models used today in the analysis of population dynamics [Goel, 1971]. Here, we employ an LV model that describes interactions between three species in an ecosystem, i.e. one predator and two preys [Mimura & Kan-on, 1986]. In addition to the predation of the preys, the two preys compete with each other for their feeding ground. The dynamics are given by

$$\tau\dot{x_1} = (1 - x_1 - cx_2 - ky)x_1, \tag{1}$$

$$\tau\dot{x_2} = (a - bx_1 - x_2 - y)x_2, \tag{2}$$

$$\tau\dot{y} = (-r + \alpha k x_1 + \beta x_2)y, \tag{3}$$

where x_1 and x_2 represent the prey population, y the predator population, τ the time constant, and the rest (k, a, b, c, r, α and β) are control parameters. The system exhibits stable, periodic and chaotic behaviors that can be controlled by single parameter r under some parameter constraints [Mimura & Kan-on, 1986].

Analog MOS circuits for LV-type neural networks have already been proposed in the literature [Asai *et al.*, 2003]. Logarithmic transformation of system variables were used to remove the multiplication terms of system variables in the LV system. In this paper, we introduce a new scaling constant in the transformation.

By introducing the following variables with scaling constant s:

$$X_1 = s + \ln x_1, \quad X_2 = s + \ln x_2, \quad X_3 = s + \ln y, \tag{4}$$

Eqs. (1)–(3) can be transformed into:

$$\tau'\dot{X}_1 = s' - \exp(X_1) - c\exp(X_2) - k\exp(Y), \tag{5}$$

$$\tau'\dot{X}_2 = as' - b\exp(X_1) - \exp(X_2) - \exp(Y), \tag{6}$$

$$\tau'\dot{X}_3 = -rs' + \alpha k\exp(X_1) + \beta\exp(X_2), \tag{7}$$

where $s' \equiv \exp(s)$ and $\tau' \equiv \tau s'$. This logarithmic transformation has two advantages in analog MOS implementation: (i) the resulting equations [(5)–(7)] do not have multiplication terms of system variables and can be described by a linear combination of exponential functions, which enables us to design the circuit without an analog multiplier; (ii) exponential nonlinearity is an essential characteristic of semiconductor devices, which enables us to design a circuit based on the intrinsic characteristics of semiconductors. Here, we use the exponential current–voltage characteristics of subthreshold MOS FETs [Vittoz, 1985; Andreou *et al.*, 1991].

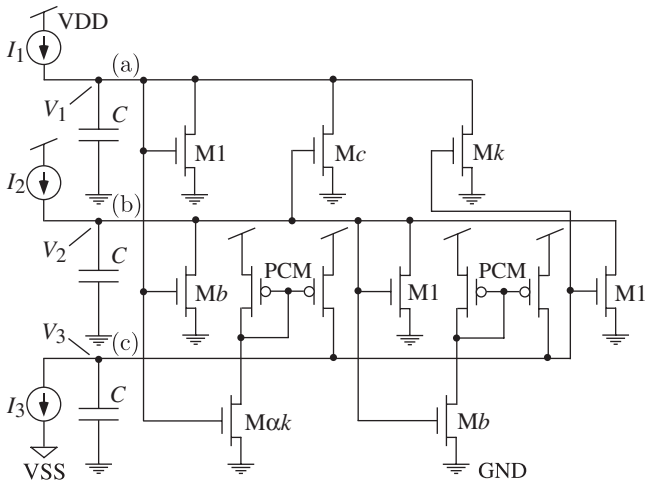


Fig. 1. Construction of the LV circuit.

Figure 1 is a diagram of the construction of an LV circuit. Applying Kirchhoff's current law (KCL) at node (a) and (b) in Fig. 1, we obtain

$$C\dot{V_1} = I_1 - I_0^{(\mathrm{M}1)}\exp\left(\frac{\kappa}{V_T}V_1\right) - I_0^{(\mathrm{M}c)}\exp\left(\frac{\kappa}{V_T}V_2\right) - I_0^{(\mathrm{M}k)}\exp\left(\frac{\kappa}{V_T}V_3\right) \tag{8}$$

$$C\dot{V_2} = I_2 - I_0^{(\mathrm{M}b)}\exp\left(\frac{\kappa}{V_T}V_1\right) - I_0^{(\mathrm{M}1)}\exp\left(\frac{\kappa}{V_T}V_2\right) - I_0^{(\mathrm{M}1)}\exp\left(\frac{\kappa}{V_T}V_3\right), \tag{9}$$

where V_i represents the node voltage, $I_{1,2}$ the injecting current, C the capacitance, κ the effectiveness of the gate potential, $V_T \equiv kT/q \approx 26\,\mathrm{mV}$ at room temperature (k is Boltzmann's constant, T temperature, and q electron charge), and $I_0^{(\mathrm{M}i)}$ the fabrication parameter of nMOS FET Mi given by

$$I_0 \equiv \mu C_{\mathrm{ox}}\frac{W}{L}\frac{1-\kappa}{\kappa}V_T^2 \tag{10}$$

where μ is the electron mobility, C_{ox} the gate capacitance, and W and L the channel width and length of MOS FETs [Vittoz, 1985]. Typical parameter values for minimum-size devices fabricated in a standard 1.5-μm n-well process are $I_0 = 0.5 \times 10^{-15}$ A and $\kappa = 0.6$. Parameter $I_0^{(\mathrm{M}i)}$ is proportional (or inversely proportional) to the channel width (or length) of MOS FETs. Since the dimensions

(width/length) are responsible for the parameters of the LV model, these must be predetermined before the IC is fabricated. It should be noted that Eqs. (8) and (9) are valid only when the MOS FETs are saturated. Node voltages V_1 and V_2 are also applied to the gates of MOS FETs Mαk and M$_\beta$, respectively. Because the currents of Mαk and Mβ are copied to node (c) by two pMOS current mirrors (PCMs in Fig. 1), the node equation is represented by

$$C\dot{V_3} = -I_3 + I_0^{(\mathrm{M}\alpha k)} \exp\left(\frac{\kappa}{V_T} V_1\right) + I_0^{(\mathrm{M}\beta)} \exp\left(\frac{\kappa}{V_T} V_2\right). \quad (11)$$

Equations (8), (9) and (11) become equivalent to Eqs. (5)–(7), respectively, when

$$V_i = \frac{V_T}{\kappa} X_i \quad (i = 1, 2, 3), \quad (12)$$

$$\frac{I_1}{I_0^{(\mathrm{M1})}} = s', \quad \frac{I_2}{I_0^{(\mathrm{M1})}} = as', \quad \frac{I_3}{I_0^{(\mathrm{M1})}} = rs', \quad (13)$$

$$\frac{I_0^{(\mathrm{M}k)}}{I_0^{(\mathrm{M1})}} = k, \quad \frac{I_0^{(\mathrm{M}b)}}{I_0^{(\mathrm{M1})}} = b, \quad \frac{I_0^{(\mathrm{M}c)}}{I_0^{(\mathrm{M1})}} = c, \quad (14)$$

$$\frac{I_0^{(\mathrm{M}\alpha k)}}{I_0^{(\mathrm{M1})}} = \alpha k, \quad \frac{I_0^{(\mathrm{M}\beta)}}{I_0^{(\mathrm{M1})}} = \beta, \quad \tau' = \frac{CV_T}{I_0^{(\mathrm{M1})}\kappa}. \quad (15)$$

With the original parameter set of the LV model [Mimura & Kanon, 1986], the values of system variables (x_1, x_2 and y) were restricted within interval $[0 : 1]$, which resulted in the extent of $(-\infty : s\, V_T/\kappa]$ V for the circuit system variables (V_1, V_2 and V_3) obtained by Eq. (12). Notice that both V_1 and V_2 cannot take negative values due to the limit of supply voltage ($V_i \geq$ GND). Furthermore, Eqs. (8) and (9) are valid only when the nMOS FETs are saturated; i.e. V_1, $V_2 \geq 4V_T \approx 0.1\,V$ at room temperature. Therefore, s ($= \ln s'$) must satisfy the condition

$$s > 4\kappa - \ln \min[x_i(t)] \quad (i = 1, 2). \quad (16)$$

With a large negative V_i ($x_i \approx 0$), this limit is negligible because $\dot{x_i} \approx 0$. Assuming that typical values for I_0 and maximum subthreshold current are $O(10^{-15})$ A and $O(10^{-7})$ A, respectively, we can estimate $s \approx 18.4$ ($= \ln 10^8$), from Eq. (13). This means that the circuit can emulate Eqs. (1) and (2) perfectly as long as $\min[x_i(t)] > 1.1 \times 10^{-7}$ (we here assumed $\kappa = 0.6$).

If we employ a nMOS transistor instead of current source I_3, on the other hand, negative V_3 breaks the isolation of pn junctions between the p-substrate and the drain of the nMOS transistor. Here, we have to employ an off-chip nMOS transistor as current source I_3.

3. Experimental Results

We fabricated a prototype circuit with a scalable complementary-MOS (CMOS) rule (MOSIS, vendor: AMIS, n-well single-poly double-metal CMOS process, $\lambda = 0.8\,\mu$m, feature size: $1.5\,\mu$m). Figure 2 is a micrograph of the LV circuit. We employed the same parameter set for the LV system ($k = 10$, $b = 1.5$, $c = 1$, $\alpha k = 5$, $\beta = 0.5$) as Mimura and Kan-on [1986] where stable focus bifurcates into chaotic oscillation via stable period-n cycles. The resulting sizes of nMOS FETs are listed in Table 1. The pMOS current mirrors (PCM) were designed with a dimension of $W/L = 4\,\mu\mathrm{m}/1.6\,\mu$m. We employed minimum size transistors for M1 and PCM to design the circuit so that it was as compact as possible, rather than compensating for device mismatches between transistors. The circuit took up a total area of $75\,\mu\mathrm{m} \times 40\,\mu$m.

Before fabrication, we simulated the operation range of variable V_3 by using ideal current source I_3. Unfortunately, V_3 took both positive and negative values when the given parameter set by Mimura

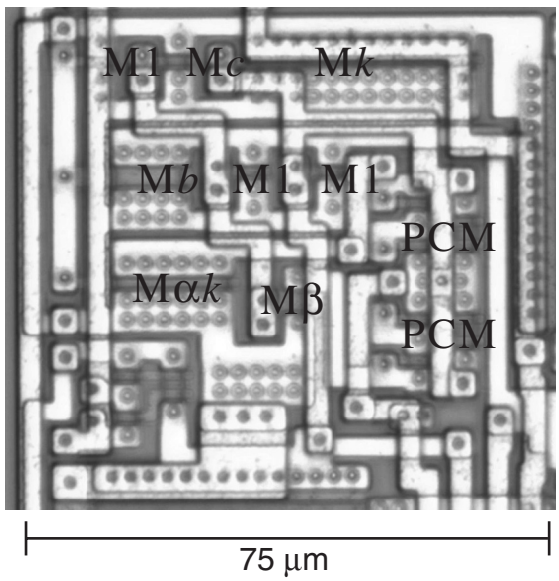


Fig. 2. Chip micrograph of a fabricated LV circuit (MOSIS, vendor: AMIS, n-well single-poly double-metal CMOS process, feature size: $1.5\,\mu$m, total area: $75\,\mu\mathrm{m} \times 40\,\mu$m).

Table 1. Designed size of nMOS FETs on LV circuit. Corresponding parameters of LV models in Eqs. (13) to (15) are $k = 10$, $b = 1.5$, $c = 1$, $\alpha k = 5$, and $\beta = 0.5$. Since $\lambda = 0.8\,\mu$m and the feature size is $1.5\,\mu$m, all the designed sizes are scaled down by $1.5\,\mu\text{m}/1.6\,\mu\text{m}$ ($\approx 94\%$) on actual chips.

MOS FET	W (μm)	L (μm)
M1	4	1.6
Mb	12	3.2
Mc	4	1.6
Mk	40	1.6
Mαk	20	1.6
Mβ	4	3.2

and Kan-on [1986] was used. Since finding a good parameter set that ensures $V_3 > 0$ is another subject altogether, we employed an off-chip current source as I_3 with the original parameter set.

In the following experiments, we added off-chip capacitors ($C = 0.1\,\mu$F) due to the time resolution of our measurement systems. The values of capacitances did not change the qualitative behaviors of the circuit, as long as the value was much larger than that of the gate capacitance of MOS transistors. We used Agilent 4156B as off-chip current sources for input (I_1, I_2 and I_3). Time courses for V_1, V_2 and V_3 were sampled simultaneously with Agilent 4156B. The supply voltage (VDD) was set at 2.5 V. The input currents (I_1, I_2) were fixed at (250, 287) nA. We evaluated the dynamic behaviors of the fabricated LV circuit by changing rest input current I_3 that corresponded to control parameter r in Eq. (3).

Figure 3 plots the measurement results. Figures 3(a) and 3(b) plot the time courses of system variables (V_1, V_2 and V_3) and trajectories on a V_1–V_3 plane, respectively. In this experiment, I_3 was

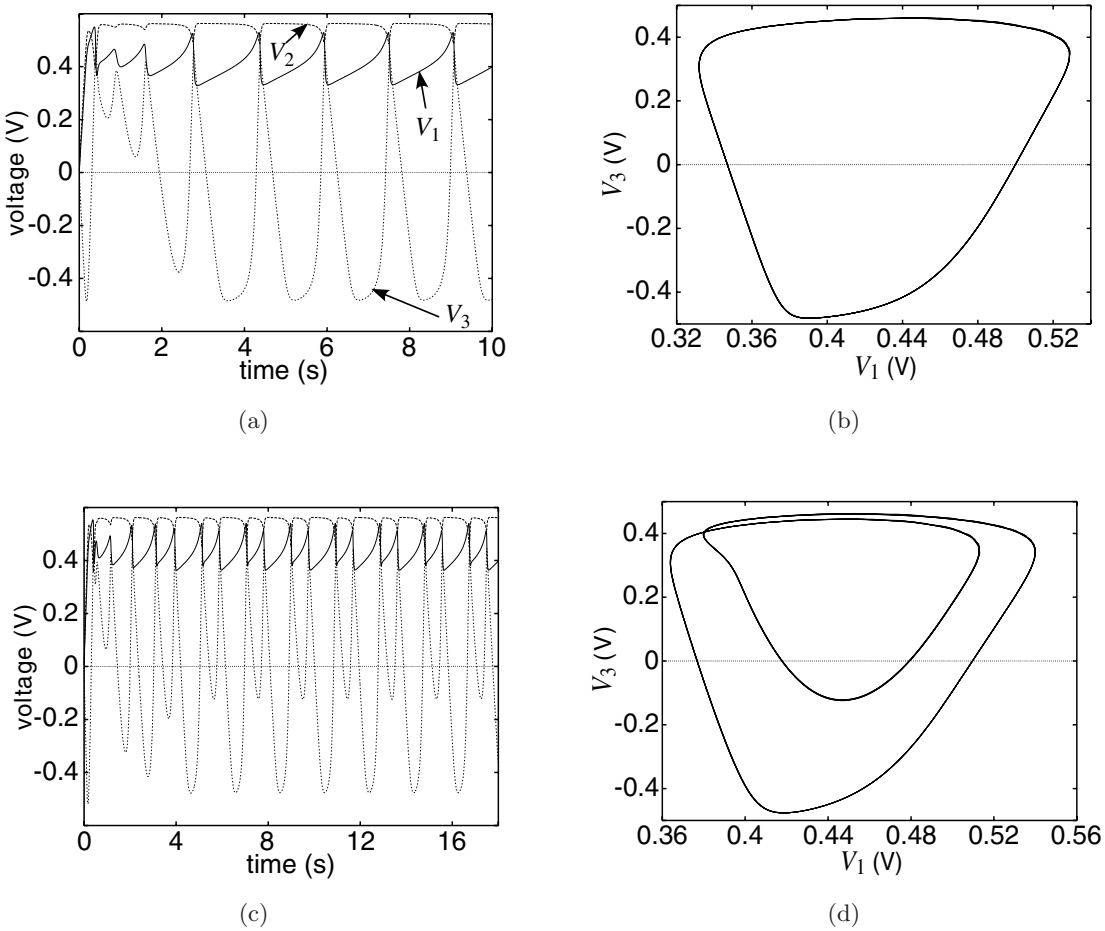
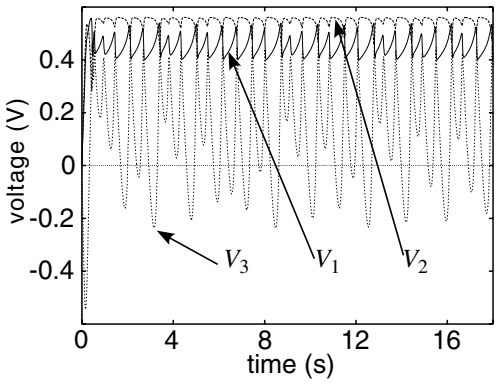
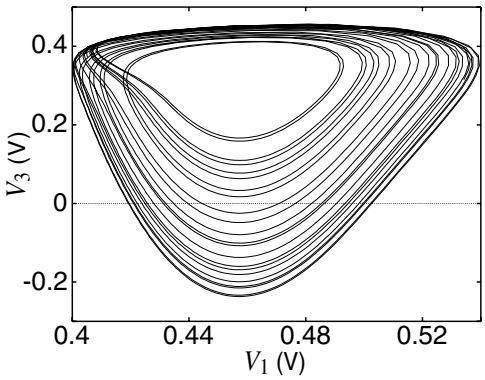


Fig. 3. Experimental results for fabricated LV circuit. (a) and (c) show time courses for system variables (V_1, V_2 and V_3). (b) and (d) show trajectories on V_1–V_3 plane. (a) and (b) represent results for $I_3 = 320$ nA, while (c) and (d) results for $I_3 = 360$ nA. (e) and (f) show time courses for system variables (V_1, V_2 and V_3) trajectories on a V_1–V_3 plane, respectively, when $I_3 = 420$ nA.



(e)



(f)

Fig. 3. (*Continued*)

set at 320 nA (compliance was set at −2.5 V). The LV circuit exhibited stable oscillation with period-1 cycles. As predicted by simulations, V_3 took positive and negative values. An off-chip current source (or nMOS transistor) is thus necessary for this circuit with the original parameter set.

In Figs. 3(c) and 3(d), which represent the time courses for system variables and trajectories on the V_1–V_3 plane, respectively, I_3 was set at 360 nA. The LV circuit exhibited stable oscillation with period-2 cycles. Figures 3(e) and 4(f) plot the time courses of system variables and trajectories on the V_1–V_3 plane, respectively. In this experiment, I_3 was set at 420 nA. The value for the maximum Lyapunov exponents was 10.1, which indicated that the LV circuit exhibited chaotic oscillation.

According to Mimura and Kan-on [1986], as the value of control parameter r increases, Hopf bifurcation occurs where stable focus bifurcates to unstable focus with an enclosing limit cycle. Then unstable focus bifurcates to stable focus. We confirmed this transition (stable focus → unstable focus with enclosing limit cycle → stable focus) in the LV circuit when I_3 ($\sim r$) increased. Figure 4 is the bifurcation diagram obtained from the LV circuit. The diagram was created as follows: (i) when the circuit had stable focus with a given I_3, we plotted a stable value for V_3, (ii) when the circuit oscillated with a given I_3, we plotted a value for V_3 at which $\dot{V}_3 = 0$. When $I_3 < 182$ nA, the LV circuit did not oscillate (stable focus). Stable focus bifurcated at $I_3 \approx 182$ nA to stable period-1 cycles. Increasing the value of I_3, further bifurcations to period-2 cycles, period-4 cycles, and chaotic cycles occurred around 370 nA $< I_3 <$ 450 nA. Finally, unstable focus bifurcated to stable focus again at $I_3 \approx 580$ nA.

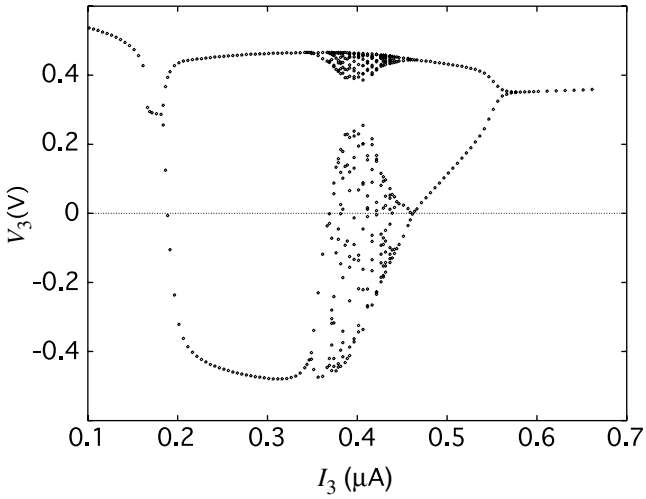


Fig. 4. Bifurcation diagram obtained from LV circuit.

The results in Fig. 4 indicate that the proposed LV circuit has two important properties: (i) although we used practical subthreshold MOS FETs, the bifurcation property was qualitatively consistent with the theoretical prediction; (ii) the LV circuit exhibited stable oscillation with period-n and chaotic cycles over a wide range of I_3; i.e. 182 nA $< I_3 <$ 580 nA, which allowed it to maintain stable oscillation under a noisy environment, even though subthreshold MOS FETs were used in the circuit.

4. Summary

We proposed an analog integrated circuit (IC) that implemented the Lotka–Volterra (LV) chaotic oscillator. We designed a very simple (just 12 transistors) circuit for the LV oscillator where all transistors operated in their subthreshold region. The

LV oscillator was fabricated with a 1.6–μm scalable CMOS rule (MOSIS, vendor: AMIS, n-well single-poly double-metal process, $\lambda = 0.8\,\mu$m, feature size: $1.5\,\mu$m). The circuit took up a total area of $75\,\mu\text{m} \times 40\,\mu\text{m}$. The qualitative behavior (bifurcation properties) agreed well with the theoretical prediction. Furthermore, the LV circuit exhibited stable oscillation with period-n and chaotic cycles over a wide range of control current, which enabled us to design a stable oscillator that could operate under a noisy environment, even though subthreshold MOS FETs were used in the circuit.

Implementing compact chaotic circuits on CMOS ICs has significant advantages; i.e. a large-scale 2D array of chaotic (nonlinear) oscillators can easily be incorporated with conventional CMOS technology. Diffusive LV systems, where each LV oscillator is locally connected through diffusive coupling, are known to produce various spatiotemporal patterns [Mimura & Kanon, 1986; Jornè, 1977; Fiasconaro *et al.*, 2004]. This property is very useful where we consider the diffusive LV system to be a reaction–diffusion (RD) computing medium [Adamatzky, 2001]. Analog ICs implementing the 2D array of LV oscillators should assist us in exploring and discovering novel RD-based applications as well as applications of nonlinear-coupled oscillators.

Acknowledgment

This study was supported by Industrial Technology Research Grant Program in '04 from New Energy and Industrial Technology Development Organization (NEDO) of Japan.

References

Adamatzky, A. [2001] *Computing in Nonlinear Media and Automata Collectives* (IOP Publishing, Bristol).

Andreou, A. G., Boahen, K. A., Pouliquen, P. O., Pavasović, A., Jenkins, R. E. & Strohbehn, K. [1991] "Current-mode subthreshold MOS circuits for analog VLSI neural systems," *IEEE Trans. Neural Networks* **2**, 205–213.

Asai, T., Kanazawa, Y. & Amemiya, Y. [2003] "A subthreshold MOS neuron circuit based on the Volterra system," *IEEE Trans. Neural Networks* **14**, 1308–1312.

Chen, G. & Ueta, T. (eds.) [2002] *Chaos in Circuits and Systems* (World Scientific, Singapore).

Elwakil, A. S. & Soliman, A. M. [1998a] "Two twin-T based op amp oscillators modified for chaos," *J. Franklin Inst.* **335B**, 771–787.

Elwakil, A. S. & Soliman, A. M. [1998b] "Two modified for chaos negative impedance converter op amp oscillators with symmetrical and antisymmetrical nonlinearities," *Int. J. Bifurcation and Chaos* **8**, 1335–1346.

Fiasconard, A., Valenti, D. & Spagnolo, B. [2004] "Nonmonotonic behavior of spatiotemporal pattern formation in a noisy Lotka–Volterra system," *Acta Physica Polonica B* **35**, 1491–1500.

Goel, S. N., Maitra, C. S. & Montroll, W. E. [1971] "On the Volterra and other non-linear models of interacting populations," *Rev. Mod. Phys.* **43**, 231–276.

Jornè, J. [1977] "The diffusive Lotka–Volterra oscillating system," *J. Theor. Biol.* **65**, 133–139.

Matsumoto, T., Chua, L. O. & Komuro, G. M. [1985] "The double scroll," *IEEE Trans. Circuits Syst-I* **CAS-32**, 798–818.

Mimura, M. & Kan-on, Y. [1986] "Predation-mediated coexistence and segregation structures," in *Patterns and Waves*: *Qualitative Analysis of Nonlinear Differential Equations*, eds. Nishida, T., Mimura, M. & Fujii, H. (Kinokuniya, Tokyo), pp. 129–155.

Radwan, A. G., Soliman, A. M. & El-Sedeek, A.-L. [2003] "MOS realization of the double-scroll-like chaotic equation," *IEEE Trans. Circuits Syst.-I* **50**, 285–288.

Sprott, J. C. [2000a] "A new class of chaotic circuit," *Phys. Lett. A* **266**, 19–23.

Sprott, J. C. [2000b] "Algebraically simple chaotic flows," *Int. J. Chaos Th. Appl.* **5**, 3–22.

Sprott, J. C. [2000c] "Simple chaotic systems and circuits," *Amer. J. Phys.* **68**, 758–763.

Vittoz, E. A. [1985] "Micropower techniques," in *Design of MOS VLSI Circuits for Telecommunications*, eds. Tsividis, Y. & Antognetti, P. (Prentice-Hall, Englewood Cliffs, NJ), pp. 104–144.