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Paper

Stochastic resonance in simple analog circuits with a single operational amplifier having a double-well potential

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Abstract: In this paper, we demonstrate *stochastic resonance* (SR) in a double-well potential system that can easily be implemented by a single operational amplifier. First, we propose a bistable mathematical model that is suitable for analog hardware implementation. Then we introduce an analog circuit for the model that is implemented by a single operational amplifier only, and demonstrate that the circuit exhibits the same SR behavior demonstrated in traditional double-well potential systems, through extensive numerical simulations and experiments.

Key Words: stochastic resonance, analog circuits, operational amplifier, double-well potential

1. Introduction

Stochastic resonance (SR) is a phenomenon where a system can stochastically detect a weak input signal with the help of noise when the input signal is below the system's threshold [1–3]. SR has been observed in many systems such as static threshold systems [4–7], monostable dynamical systems [8, 9], and bistable dynamical systems (double-well potential systems) [10, 11]. Moreover, SR has been demonstrated on electrical systems such as threshold circuits [12–15], bistable circuits [16–20], a semiconductor laser [21–23], and so on. SR may be utilized for weak signal detection in electric circuits [3, 6, 7], whereas SR in double-well electronic systems, *i.e.*, bistable electronic systems, can be used not only for weak signal detection, but also for logic memories.

Noise-driven logic memory circuits (SR memory circuits) would be valuable when the supply voltage of the circuit is extremely low. Because electric power consumption of digital circuits is proportional to the square of the supply voltage, decreasing the supply voltage is very effective to reduce power consumption. However, decreasing the supply voltage causes data writing to fail or stored data to be lost due to threshold deviation of MOS FETs. If the threshold deviation becomes the dominant factor, SR would decrease memory cell's failure rates. When threshold deviation disturbs data writing, noise may stochastically decrease the potential barrier of double-well potential of a memory cell, and the data writing would succeed. Noise sources exist everywhere. For instance, power supply noise in LSIs [24] may be used as a noise source.

Memory cells must be designed with minimal size in many functional digital systems. The most

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widely used memory cell is a latch-based circuit composed of two inverters and transfer gates. In order to construct an SR memory cell based on standard latch circuits, obtaining potential function of the latch circuit is required to evaluate SR characteristics. However, obtaining the potential function is not easy because i) ultralow supply voltage causes subthreshold operation of MOS FETs, and ii) output of a subthreshold latch circuit is represented by an unsolvable (nested) inverse function of sum of exponential functions. Hence, we propose a mathematical model whose potential function can theoretically be obtained, and construct an electric circuit which is equivalent to the latch circuit.

2. The model

Let us start by introducing the following dynamics,

$$\tau \frac{du}{dt} = -u + f_\beta(u - I), \tag{1}$$

where u represents the state variable; $f_\beta(\cdot)$, the sigmoid function whose slope factor is β; τ, the time constant; and I, the external input. Suppose that β is large enough, so $u \to 1$ when $u > I$, wheareas $u \to 0$ when $u < I$. Thus one can be convinced that this system is a bistable system ($u \to 0$ or 1).

Next, potential function of this system H will be given. When the following condition,

$$\frac{\partial H}{\partial t} = \frac{du}{dt} \cdot \frac{\partial H}{\partial u} < 0, \tag{2}$$

is satisfied, the system is considered to be stable. One can easily notice that

$$\frac{\partial H}{\partial u} = -\tau \frac{du}{dt}, \quad \text{where } \tau > 0, \tag{3}$$

is a candidate that satisfies the condition. By substituting Eq. (1) to the equation above, we obtain

$$\frac{\partial H}{\partial u} = u - f_\beta(u - I). \tag{4}$$

Integrating this by u leads to the following potential function,

$$H = \frac{1}{2}u^2 - \frac{1}{\beta}\ln\bigl(\exp(\beta u) + \exp(\beta I)\bigr) + C, \tag{5}$$

where C represents the integral constant.

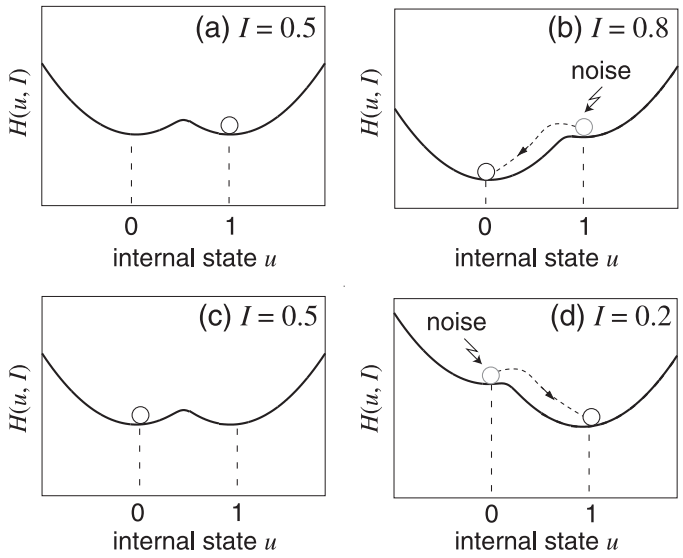

Fig. 1. Shape of potential function of proposed double-well system for different magnitudes of input I. Steady state [(a) and (c)] and possible noise-driven state transition [(b) and (d)] are depicted.

Figure 1 plots the obtained double-well potential function ($\beta = 20$ and $C = 0$) for several values of I. In the following, let us assume that i) the model accepts a periodic input, *e.g.*, $I = 0.5 + A_0 \sin(\omega t) + n(t)$, where A_0 is the amplitude; ω, the angular frequency; t, the time; and $n(t)$, the Gaussian white noise, and ii) $A_0 = 0.3$ and $n(t) = 0$ for the time being. Figure 1(a) plots an initial shape of H for $I|_{t=0} = 0.5$. When we assume $u|_{t=0} = 1$, this state ($u = 1$) is stable because it is trapped in the right well, as shown in Fig. 1(a). As time increases (I increases), the left well goes down. Figure 1(b) illustrates the lowermost case for $\omega t = \pi/2$ ($I = 0.8$). Since the middle potential barrier disappears when $I = 1$, state transition ($u = 1 \rightarrow 0$) does not occur in this example. Figure 1(c) illustrates the shape of H for the subsequent state ($\omega t = \pi$, $I = 0.5$). As time further increases, the right well goes down. Figure 1(d) illustrates the lowermost case for $\omega t = 3\pi/2$ ($I = 0.2$) where state transition does not occur as well because the middle potential barrier disappears when $I = 0$.

Consequently, when $n(t) = 0$, state transition does not occur if a subthreshold input ($A_0 < 0.5$; $0 < I < 1$) is given to the system. However, a "stochastic transition" may be caused by subthreshold inputs with nonzero $n(t)$. Small amounts of noise cannot cause the transition, whereas excessive amounts of noise may cause random transition. Therefore, one may expect that there exist optimal strength of noise that maximizes the SNR of state transition [1].

3. Circuit implementation of proposed bistable system

The double-well potential system proposed in the previous section was implemented in electric circuits with one operational amplifier only. A general operational amplifier accepts two voltage inputs (V_+ and V_-, for example) and it amplifies the voltage difference between V_+ and V_- with gain A_v. The output $A_v \cdot (V_+ - V_-)$ is clamped at supply voltages ($V_{\rm dd}$, $V_{\rm ss}$). Thus, when the gain is large enough and $V_{\rm ss} = 0$, the amplifier's output is approximated by $V_{\rm dd} \cdot \theta(V_+ - V_-)$, where $\theta(\cdot)$ is the step function.

Suppose the time constant τ in Eq. (1) is small enough, then we obtain $u \approx f_\beta(u - I)$ from Eq. (1). When β is large enough, we can say $f_\beta(\cdot) \approx \theta(\cdot)$. When we consider $V_{\rm out}$ as $u \cdot V_{\rm dd}$ and $V_{\rm in}$ as $I \cdot V_{\rm dd}$, we obtain the approximate equation; $V_{\rm out} \approx V_{\rm dd} \cdot \theta(V_{\rm out} - V_{\rm in})$. The right side of the equation is equal to the estimated output voltage of the amplifier where "V_+" node is connected to $V_{\rm out}$ and "V_-" node is connected to $V_{\rm in}$. Thus, by connecting the output node of the amplifier and "V_+" node, the system for Eq. (1) is implemented in electric circuits. Note that the circuit is extremely simple as compared with double-well potential electronic systems proposed in [16–20].

4. Results

4.1 Numerical simulation results

Numerical simulations of the proposed model given by Eq. (1) were carried out by using the following parameters; $\tau = 10^{-3}$, $\beta = 20$, $I = 0.5 + A_0 \cdot \sin(2\pi f_0 t) + n(t)$, where $A_0 = 0.2$, $f_0 = 1$ Hz, and

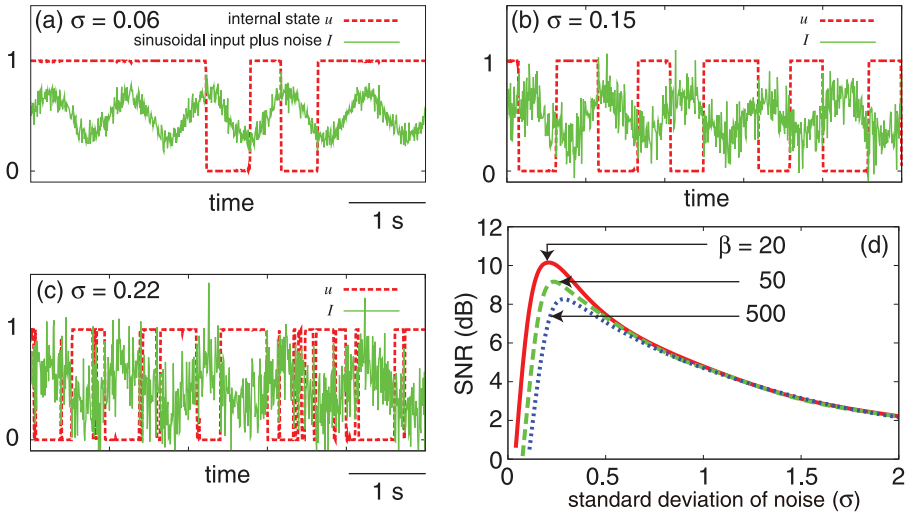

Fig. 2. Numerical simulation results exhibiting SR in proposed system.

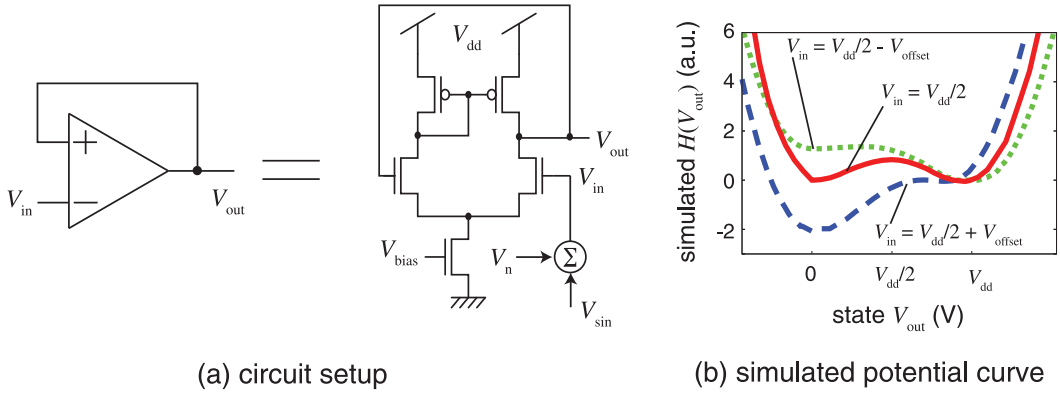

Fig. 3. Circuit setups (a) and shape of simulated potential curve of proposed circuit (b).

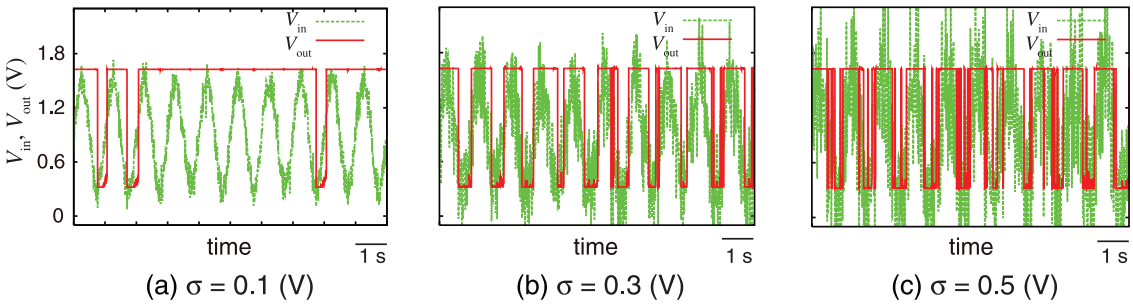

Fig. 4. Simulated transient responses of proposed circuit for subthreshold inputs with noise.

$n(t)$ is the Gaussian white noise (filtered at 100 Hz) with standard deviation σ. Figure 2 shows time courses of u and I for $\sigma = 0.06$, 0.15, and 0.22. When $\sigma = 0.06$, the rate of transition was low because the probability of disappearance of the potential barrier was low, as well [Fig. 2(a)]. As shown in Fig. 2(b), when σ was increased ($= 0.15$), state transition occurred in response to the increase and decrease of the sinusoidal input; *i.e.*, state transition of $u \to 0$ and $u \to 1$ occurred when I was high and low, respectively. For larger σ, random transition of u was observed because the sinusoidal input was buried in noises [Fig. 2(c); $\sigma = 0.22$]. Figure 2(d) plots σ versus signal-to-noise ratio (SNR) ($\equiv 10 \log_{10} S(f_0)/B(f_0)$ where $S(f_0)$ and $B(f_0)$ represent the signal and background level at f_0 in the power spectra of u), with several values of β. When $\beta = 20$, the peak SNR was 10.5 dB at $\sigma = 0.2$. For larger β (50 and 500), the peak SNR was decreased because large β elevate the potential barrier, which result in blocking noise-driven state transition in response to the subthreshold input.

4.2 SPICE simulation results

Figure 3(a) illustrates the simulation setups. In the following simulations, we used a standard 0.18-μm CMOS parameter set (minimum W/L of transistors for analog simulations) with $V_{\rm dd} = 1.8$ V and $V_{\rm bias} = 0$ V. Figure 3(b) shows potential curves of the proposed circuit ($V_{\rm offset} = 0.3$ V). The potential curves were obtained by integrating simulated transient data ($dV_{\rm out}/dt$) by $V_{\rm out}$ with four different initial conditions; *i.e.*, $V_{\rm out}|_{t=0} < 0$, $V_{\rm out}|_{t=0} = V_{\rm dd}/2 - \Delta V$ ($\Delta V \ll 1$), $V_{\rm out}|_{t=0} = V_{\rm dd}/2 + \Delta V$, and $V_{\rm out}|_{t=0} > V_{\rm dd}$.

Figure 4 shows transient simulation results of the proposed circuit. In the simulations, we used $V_{\rm in} = V_{\rm n} + V_{\rm sin}$ where $V_{\rm n}$ is the Gaussian white noise (filtered at 100 Hz) with standard deviation σ, and $V_{\rm sin} = V_{\rm dd}/2 + A_0 \sin(2\pi f t)$ ($A_0 = 0.6$ V; $f = 1$ Hz). The Gaussian noise sequence was externally generated and was included in the SPICE codes as a PWL voltage source. Figures 4(a), (b), and (c) represent the inputs ($V_{\rm in}$) and outputs ($V_{\rm out}$) of the system with $\sigma = 0.1$, 0.3, and 0.5 V, respectively. The results were qualitatively equivalent to numerical simulation results shown in Figs. 2(a) to (c); *i.e.*, i) small σ could not induce stochastic transition sufficiently, ii) moderate σ induced state transition in response to the input, and iii) large σ caused random state transition.

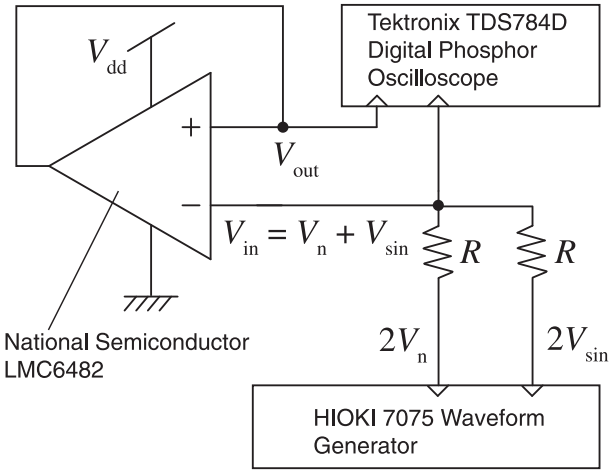

Fig. 5. Electric circuit having using Double-well potential using single operational amplifier.

Hence, one may observe SR behaviors with the proposed circuit consisting of "single" operational amplifier.

4.3 Experimental results

Figure 5 shows our experimental configuration. A CMOS full-swing (Rail-To-Rail) operational amplifier (National Semiconductor, LMC6482) was used and supply voltage $V_{\rm dd}$ was set to 3 V. A input signal applied to the amplifier was $V_{\rm in} = V_{\rm sin} + V_{\rm n}$, where $V_{\rm sin}$ the sinusoidal input and $V_{\rm n}$ the noise voltage. $V_{\rm in}$ was generated by a resistive voltage divider ($R = 1$ kΩ)[1]. $V_{\rm in}$ was applied to "–" node of the operational amplifier(an input node of the proposed circuit). Furthermore, $V_{\rm sin}$ was given by $V_{\rm offset} + V_0 \cdot \sin(2\pi f_0 t)$, where $V_{\rm offset}$ was 1.5 V, V_0 was 1 V, and f_0 was 200 Hz. $V_{\rm n}$ was the time varying Gaussian noise voltage whose average and standard deviation were 0 V and σ V. Both $V_{\rm sin}$ and $V_{\rm n}$ were given by a waveform generator (HIOKI, 7075). Pseudo-random sequences were generated by using the Box-Muller method from a computer simulation. $V_{\rm n}$ was the Pseudo-random sequence that was imported to the waveform generator with frequency limitation of 19 kHz. We observed waveforms of the input and output voltages ($V_{\rm in}$ and $V_{\rm out}$) by an oscilloscope (Techtronix, TDS784D) and sampling rate was 100 kHz . We also observed power spectrum of the output voltage ($V_{\rm out}$) by a FFT module, which is equipped with the oscilloscope (averaged over 1000 times in frequency domain), and obtained SNR by subtracting the background noise level on f_0 from the signal level on f_0.

Figure 6 shows experimental results (waveform screens of the oscilloscope) where σ was set to 0.3 V, 0.75 V, and 1.5 V. Each figure, (a), (b), and (c), contains time courses of $V_{\rm in}$ (upper), time courses of $V_{\rm out}$ (middle), and power spectrum of $V_{\rm out}$ (lower). When $\sigma = 0.3$ V, probability of $V_{\rm out}$ transition was small [Fig. 6(a)]. Because the offset and amplitude of $V_{\rm sin}$ were 1.5 V and 2 $V_{\rm pp}$ ($V_{\rm sin} = 0.5$–2.5 V), the minimal voltage of $V_{\rm n}$ for transitions from '1' to '0' and from '0' to '1' are +0.5 V (when $V_{\rm sin}$ is 2.5 V) and −0.5 V (when $V_{\rm sin}$ is 0.5 V), respectively. This indicates that when σ were 0.3 V, a possibility of $V_{\rm n} > 0.5$V (or $V_{\rm n} < -0.5$ V) and the transition possibility were small [Fig. 6(a)]. We measured signal and background level at 200 Hz in power spectrum and found that SNR was 6.4 dB. When $\sigma = 0.75$ V, possibility of $V_{\rm n} > 0.5$V (or $V_{\rm n} < -0.5$V) was higher than the transition possibility of $\sigma = 0.3$ V, and transition possibility was also higher [Fig. 6(b)]. The SNR in this case was 21.5 dB. The important fact is that the possibility of the transition from 0 to $V_{\rm dd}$ became high when $V_{\rm sin}$ is low, and the possibility of the transition from $V_{\rm dd}$ to 0 became high when $V_{\rm sin}$ was high. In other

[1]Upon the experiments (with large σ), one should pay attention to voltage amplitudes of the amplifier's inputs; *i.e.*, R should significantly be larger than "on" resistance ($R_{\rm on}$) of electrostatic discharge (ESD) diodes (for MOS gate protection) in the CMOS operational amplifier (LMC6482). When the amplifier's input "V_+" (or "V_-") exceeds $V_{\rm dd}$ (or falls below $V_{\rm ss}$), the diodes are forwardly biased, which results in large (shunting) currents on the ESD paths. To avoid this, we employed a resistive voltage divider, as shown in Fig. 5. As long as $2R_{\rm on}/R \approx 0$ ($R \gg R_{\rm on}$), $V_{\rm in}$ does not exceed $V_{\rm dd}$ (or does not fall below 0) significantly, when $V_{\rm n} + V_{\rm sin}$ exceeds $V_{\rm dd}$ (or falls below 0). Namely, the excess voltage drops across R.

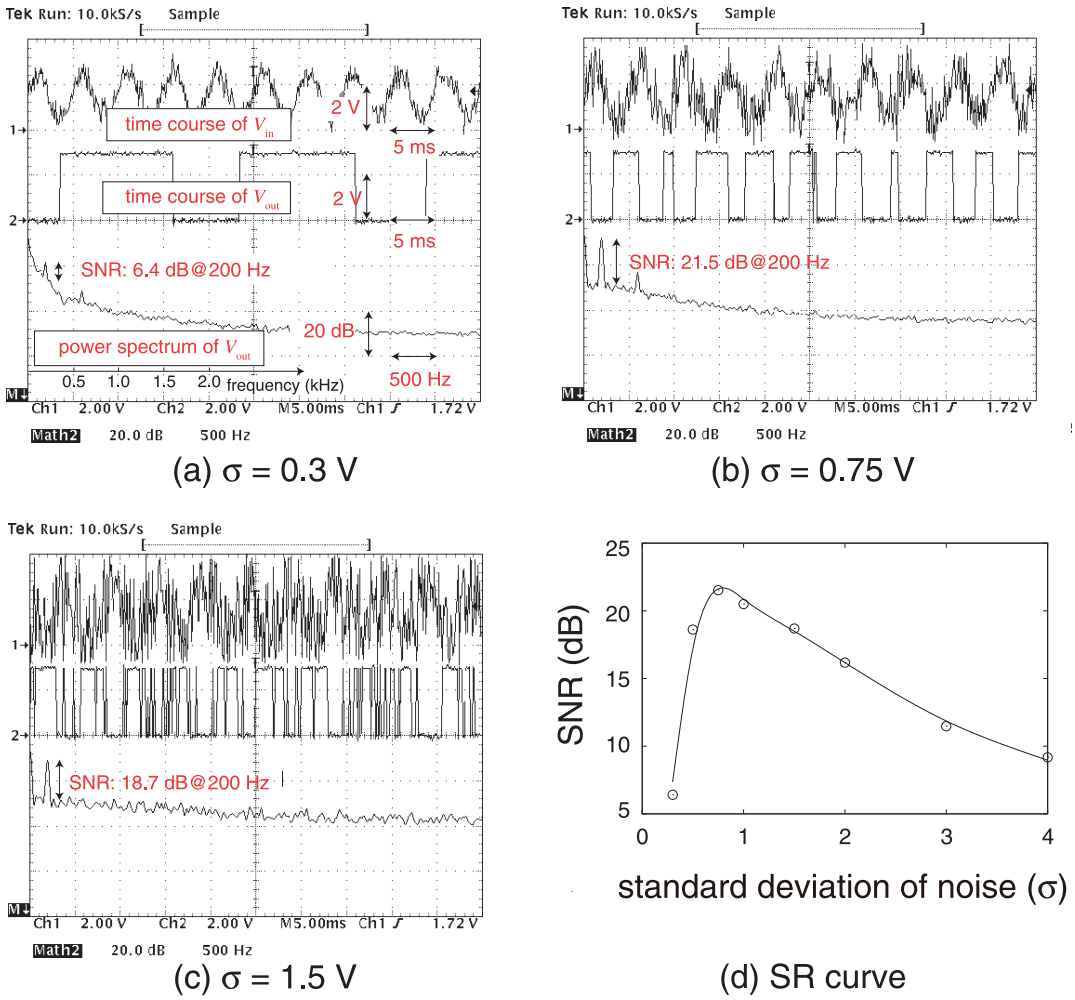

Fig. 6. Experimental results of proposed circuit. (a)–(c) time courses of input $V_{\rm in}$ (top waveform), output $V_{\rm out}$ (middle), and power spectrum of $V_{\rm out}$ (bottom) for $\sigma = 0.3$ V, 0.75 V, and 1.5 V; (d) SR curve (SNR versus σ) of proposed circuit.

words, although $V_{\rm sin}$ didn't have the amplitude required for the transition, the noise stochastically helped the transition of $V_{\rm out}$ to $V_{\rm dd}$ (or 0) depending on $V_{\rm sin}$. The experimental results in $\sigma = 1.5$ V are shown in Fig. 6(c). In this case, the SNR was 18.7 dB. The SNR didn't decrease suddenly as it seems, but the frequent transition of $V_{\rm out}$ occurred. This is because the noise level almost always surpassed the signal level required for transition. Figure 6(d) shows the experimental SNR curve that was obtained by varying standard deviation of noise σ from 0 to 4 V. The maximum SNR was 21.5 dB ($\sigma = 0.75$ V).

5. Discussion

As described in Section 1, SR in bistable system could be utilized in logic memory systems. In this paper, to obtain a theoretical potential function, we designed a bistable circuit with an operational amplifier. However, the amplifier requires constant bias currents, which results in dissipating power even in the steady state. Hence, one should use standard (inverter-based) latch circuit that does not dissipate power in the steady state, if one aims at practical applications of SR in low-power memory systems.

Let us suppose that the power-supply voltage of a standard latch circuit is extremely decreased, aiming at the ultra-low power operation. One may easily find that there exists the lower limit for correct memory operations (writing and storing operations) due to the transistor's mismatch. What happens if we use multiple (but unstable due to the mismatch) latch circuits driven by noise, and do majority voting among N latch circuits to represent 1 bit data? SR helps to improve incorrect

writing and storing operations stochastically. Power dissipation of the larch array would be N times larger than that of a single latch (the power is linearly increased as N increases), whereas power of digital circuits is proportional to the square of the power-supply voltage. Hence, we conclude that i) SR improves bit-error rate of an array of latch circuits with extremely low-power-supply voltage as N increases, ii) the power dissipation is determined by the required (capable) bit-error rate, and iii) if a certain degree of error is accepted, an SR-based memory system may drastically decrease the total power dissipation.

6. Summary

To observe stochastic resonance (SR) in an electronic bistable system, we proposed a double-well potential system that can easily be implemented by a single operational amplifier. We first obtained a potential function of the system and its bistable conditions. Then, we constructed a simple electric circuit based on the system. The circuit is extremely simple as compared with double-well potential electronic systems proposed in [16–20]. We conducted numerical and SPICE simulations as well as experiments of the circuit. We confirmed the same SR behavior observed in conventional double-well potential systems [1].

Acknowledgments

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