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Low-power temperature-to-frequency converter consisting of subthreshold CMOS circuits for integrated smart temperature sensors

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ABSTRACT

A low-power temperature-sensing oscillator was developed using a 0.35-μm standard CMOS process. This oscillator generates a clock pulse whose frequency is proportional to absolute temperature (PTAT frequency). It consists of a PTAT current generator controlled with an external reference clock and a frequency-locked loop biased with an external reference voltage. The PTAT current generator makes use of the exponential current characteristic of MOSFETs operated in the subthreshold region. Theoretical analyses and experimental results showed that the circuit can be used as a temperature sensor with a low-power consumption of 10 μW or less. The temperature coefficient of the output frequency was insensitive to variation in device parameters, so the sensor circuit can be used only with one-point calibration. Its temperature-sensing error was from −1.8 to +1 °C in a temperature range of 10–80 °C. This temperature sensor would be suitable for use in subthreshold-operated, power-aware LSIs.

1. Introduction

In the near future, intelligent network systems with various smart-sensor devices are expected to be developed and spread all over the world to enable infrastructures to be constructed for the information age. Such network systems require a huge number of sensor devices that measure various physical data in our surroundings, store and process the measured data, and output the data on demand. Such sensors must operate for a long time with scant energy resources such as micro-sized batteries and energy-harvesting devices; thus, to improve their overall efficiency, reducing their energy consumption is inevitable [1]. One promising method of reducing energy consumption is to make the sensors with CMOS circuits that operate in the subthreshold region of MOSFETs, i.e., a region in which the gate-source voltage of MOSFETs is lower than the threshold voltage [2,3]. As a step toward such sensor LSIs, we have focused on smart temperature-sensor LSIs (for our previous work on subthreshold-operated CMOS sensors, see [4]) and developed an ultra-low power sensor that can operate with a dissipation of 10 microwatts or less. The following sections provide the details of this sensor.

Many smart temperature sensors have been reported. Most integrated temperature sensors make use of the temperature dependence of CMOS-based vertical bipolar transistors [5–10]. These sensors can generate accurate sensing signals stably. Other temperature sensors using the temperature dependence of MOSFETs have been reported [11–14]. These sensors are low-power dissipations, about less than 100 μW. However, their sensing signals require two-point calibration because of nonlinearity in the signal. Therefore, a trade-off exists between power dissipation and temperature inaccuracy. For simplicity of measurements and reduction in production costs of sensors, the calibration method should be one-point calibration.

To solve these problems, we developed a new temperature sensor device that can operate with sub-10-microwatt power dissipation and uses only one-point calibration technique. Our sensor consists of subthreshold CMOS circuits and uses a frequency-locked loop technique. It generates a clock output with a frequency proportional to absolute temperature (PTAT frequency). One-point calibration suffices for correct operation because the temperature coefficient of the sensor is insensitive to process variations. The following sections provide the details on our temperature sensor. Section 2 describes the principle of our sensor and discusses the effect of temperature and process variations. Section 3 presents the characteristics of a prototype that was fabricated by using 0.35-μm standard CMOS process technology. The device showed a temperature inaccuracy within −1.8 to +1 °C and a low-power dissipation of 10 μW or less [15].

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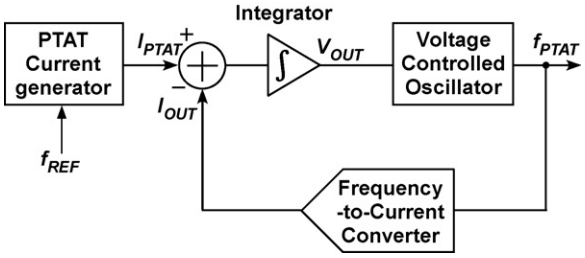

Fig. 1. Block diagram of PTAT clock generator.

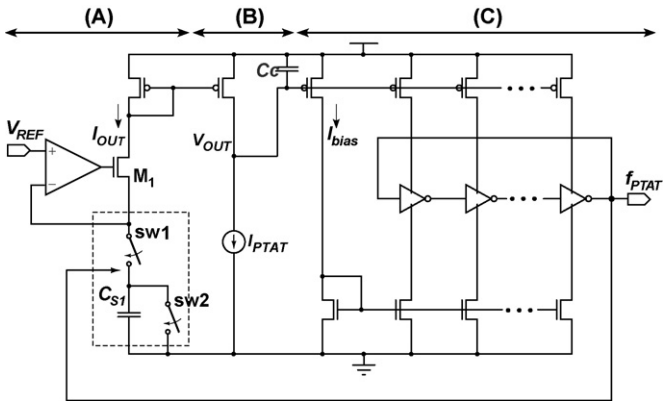

Fig. 2. Construction of PTAT clock generator.

2. Circuit configuration

Fig. 1 shows a block diagram of our temperature sensor, which generates a PTAT clock frequency using a frequency-locked loop technique. It consists of a PTAT current generator controlled with an external reference clock f_{REF}, a current subtractor, a integrator, a voltage-controlled oscillator (VCO), and a frequency-to-current converter. The current subtractor, integrator, VCO, and frequency-to-current converter form a feedback loop. The current subtractor detects the difference between output current I_{PTAT} of the PTAT current generator and output current I_{OUT} of the frequency-to-current converter. Then, the integrator integrates the difference of the two currents, so the voltage V_{OUT} of the integrator is proportional to the difference between I_{PTAT} and I_{OUT}. The VCO accepts V_{OUT} and produces oscillation pulses with frequency f_{PTAT} as a function of V_{OUT} of the integrator. The frequency-to-current converter accepts the oscillation pulses and generates I_{OUT} that is proportional to f_{PTAT}. The current subtractor again compares I_{OUT} with I_{PTAT} to produce readjusted V_{OUT}. This feedback operation is repeated to make I_{OUT} equal to I_{PTAT}. Resultant clock frequency f_{PTAT} is proportional to absolute temperature. Fig. 2 shows the construction of the temperature-sensor circuit. Subcircuit (A) is the frequency-to-current converter, subcircuit (B) is the current subtractor and the integrator, I_{PTAT} in subcircuit (B) is provided by the PTAT current generator, and subcircuit (C) is the VCO. All MOSFETs in the circuit are operated in the subthreshold region to achieve low-power consumption. The following sections describe the operation of the sensor circuit in detail.

2.1. Operation principle

2.1.1. PTAT current generator

Fig. 3 shows the PTAT current generator. The circuit is based on a β multiplier self-biasing circuit consisting of a switched capacitor instead of an ordinary resistor. The configuration of this circuit is the same as described in [16], where the circuit is used as a constant-Gm biasing circuit operated in the strong inversion region of MOSFETs. In our sensor, however, the circuit is operated in the subthreshold region to obtain a PTAT current output. The switched capacitor circuit consists of capacitor C_{S2} and two switches (sw3 and sw4) driven by an external reference clock with frequency f_{REF}. It operates as a resistor with average resistance R_{SC}, which is equal to $(C_{S2} \cdot f_{REF})^{-1}$ between the source node of transistor M_2 and ground. Therefore, adjusting an external reference clock with frequency f_{REF}, resistance of the switched-capacitor resistor R_{SC} can be enlarged. Consequently, the circuit is operated with an ultra-low current, several hundred of nanoamperes or less, and transistors M_1 and M_2 are operated in the subthreshold region.

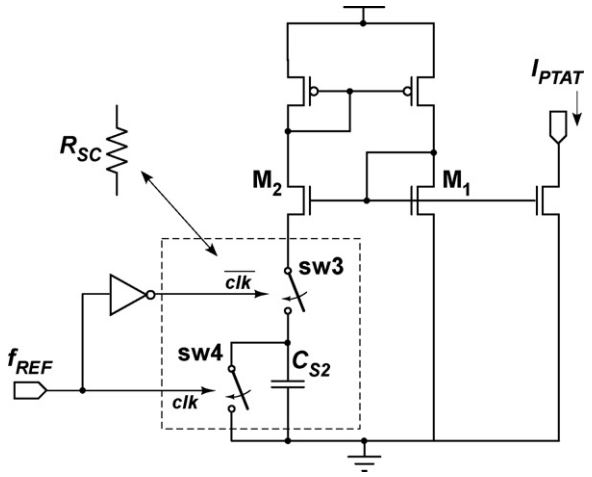

Fig. 3. PTAT current generator, consisting of subthreshold-operated MOSFETs and switched-capacitor resistor.

The subthreshold drain current I_D of a MOSFET is an exponential function of the gate-source voltage V_{GS} and the drain-source voltage V_{DS}, and given by

$$I_D = KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right)\left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right), \quad I_0 = \mu C_{OX}(\eta - 1){V_T}^2, \tag{1}$$

where K is the aspect ratio ($= W/L$) of the transistor, μ is the mobility of carriers, C_{OX} is the gate-oxide capacitance, $V_T (= k_B T/q)$ is the thermal voltage, k_B is the Boltzmann constant, T is temperature, q is the elementary charge, V_{TH} is the threshold voltage of a MOSFET, and η is the subthreshold slope factor [2,17]. For $V_{DS} > 0.1$ V, current I_D is almost independent of V_{DS} and given by

$$I_D = KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right). \tag{2}$$

In the circuit in Fig. 3, gate-source voltage V_{GS1} in M_1 is equal to the sum of gate-source voltage V_{GS2} in M_2 and voltage drop ($I_{PTAT} \cdot R_{SC}$) across the switched-capacitor resistor, i.e.,

$$V_{GS1} = V_{GS2} + I_{PTAT}R_{SC}. \tag{3}$$

Currents in M_1 and M_2 are equal, so the output current I_{PTAT} of the PTAT current generator is given by

$$I_{PTAT} = \frac{\eta V_T \ln(K_2/K_1)}{R_{SC}} = f_{REF} \cdot C_{S2} \cdot \frac{\eta k_B T}{q} \ln\left(\frac{K_2}{K_1}\right). \tag{4}$$

Because external reference clock with frequency f_{REF} is independent of temperature, output current I_{PTAT} is proportional to temperature. Thus, we can obtain a PTAT current for use of the current subtractor.

2.1.2. Current subtractor and integrator

Subcircuit (B) in Fig. 2 is the current subtractor and the integrator consisting of capacitor C_C. The current subtractor is used to

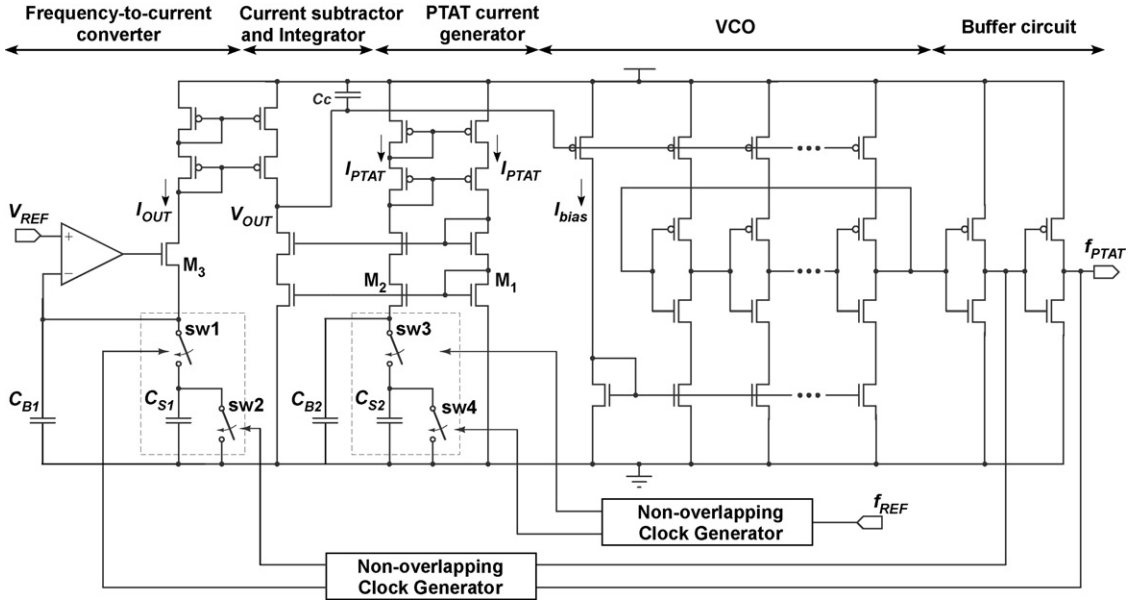

Fig. 4. Entire circuit for PTAT clock generator. All subcircuits are operated in subthreshold region.

detect the difference between I_{PTAT} produced by the PTAT current generator and output current I_{OUT} of the frequency-to-current converter. The integrator is used to integrate the difference between the two currents. Therefore, the resultant voltage V_{OUT} of the integrator is proportional to the difference between the two currents. Capacitor C_C of the integrator forms the loop filter of the frequency-locked loop and provides stability to the loop.

2.1.3. Voltage-controlled oscillator

The VCO (subcircuit (C) in Fig. 2) consists of a current-starved ring oscillator that is operated in the subthreshold region of MOSFET. The circuit is used for producing oscillation pulses that are dependent on output voltage V_{OUT} of the integrator. Oscillation frequency f_{PTAT} depends on bias current I_{bias} that is controlled by V_{OUT}, and is given by

$$f_{PTAT} = \frac{I_{bias}}{2mAC_L V_{DD}} = \frac{I_0}{2mAC_L V_{DD}} \exp\left(\frac{V_{DD} - V_{OUT} - V_{TH}}{\eta V_T}\right), \quad (5)$$

where m is the number of inverters in the oscillator, C_L is the load capacitance for each inverter, A is a delay fitting parameter [18]. Therefore, oscillation frequency f_{PTAT} depends on the output voltage V_{OUT} of the integrator.

2.1.4. Frequency-to-current converter

Subcircuit (A) in Fig. 2 shows the frequency-to-current converter. The circuit produces output current I_{OUT} that is proportional to oscillation frequency f_{PTAT} of the VCO. The voltage of one end of the switched-capacitor resistor (C_{S1} and two switches sw1 and sw2) is fixed to voltage V_{REF} with an operational amplifier, where V_{REF} is supplied by an external reference voltage such as a bandgap reference circuits. The switched-capacitor resistor is driven by the oscillation pulses from the VCO, and it operates as a resistor with a resistance of $(C_{S1} \cdot f_{PTAT})^{-1}$. Therefore, output current I_{OUT} is given by

$$I_{OUT} = f_{PTAT} \cdot C_{S1} \cdot V_{REF}. \quad (6)$$

This current is copied into the current subtractor through a current mirror. Because of the feedback operation, the circuit operates so that the output current I_{OUT} will be equal to PTAT current I_{PTAT} (i.e., Eq. (4) = Eq. (6)). Consequently, oscillation frequency f_{PTAT} will be

$$f_{PTAT} = \frac{C_{S2}}{C_{S1}} \cdot \frac{f_{REF}}{V_{REF}} \cdot \frac{\eta k_B T}{q} \ln\left(\frac{K_2}{K_1}\right). \quad (7)$$

Because we assume f_{REF} and V_{REF} as an external reference clock (e.g., crystal oscillators or clock reference generators) and voltage (e.g., bandgap reference circuits) that are independent of temperature, output frequency f_{PTAT} has a PTAT characteristic. By adjusting C_{S1}, C_{S2}, V_{REF}, and f_{REF}, the temperature coefficient (T.C.) of the PTAT current can be controlled.

2.1.5. Entire configuration

Fig. 4 shows the entire construction of the temperature sensor. The VCO consists of seven current-starved inverters connected in a ring. Non-overlapping clock pulses are used for driving the switched capacitors in the PTAT current generator and the frequency-to-current converter in order to prevent simultaneous shorting of switches. Capacitors C_{B1} and C_{B2} remove high-frequency noise caused by the switching operation. The aspect ratios of K_1 and K_2 for transistors M_1 and M_2 were set to 1:10 (i.e., M_1: W/L = 30 μm/3 μm(=(3 μm/3 μm) ×10), M_2: W/L = 300 μm/3 μm(=(3 μm/3 μm) ×100)).

2.2. Process variation

Let us consider the effect of process variation on PTAT current I_{PTAT} and output frequency f_{PTAT}. Process variation will cause two parameter variations in the circuit. First, it causes the mismatch ΔV_{TH} ($= V_{TH1} - V_{TH2}$) between the threshold voltages of M_1 and M_2 in the PTAT current generator. Second, process variation causes variation in capacitances C_{S1} and C_{S2} of the switched capacitors. Given threshold mismatch ΔV_{TH}, the PTAT current (see Eq. (4)) is rewritten as

$$I_{PTAT\_VARI} = f_{REF} \cdot C_{S2} \cdot \frac{\eta k_B T}{q} \ln\left(\frac{K_2}{K_1}\right) + f_{REF} \cdot C_{S2} \cdot \Delta V_{TH} = I_{PTAT} + f_{REF} \cdot C_{S2} \cdot \Delta V_{TH}. \quad (8)$$

The right side of Eq. (8) has an additional term due to mismatch ΔV_{TH}. Therefore, process variation will cause an offset in the output current. In addition, variation in capacitance C_{S2} will cause the variation in the T.C. of the PTAT current.

The output frequency (see Eq. (7)) including process variation is rewritten as

$$f_{PTAT\_VARI} = \frac{C_{S2}}{C_{S1}} \cdot \frac{f_{REF}}{V_{REF}} \cdot \frac{\eta k_B T}{q} \ln\left(\frac{K_2}{K_1}\right) + \frac{C_{S2}}{C_{S1}} \cdot \frac{f_{REF}}{V_{REF}} \cdot \Delta V_{TH} = f_{PTAT} + \frac{C_{S2}}{C_{S1}} \cdot \frac{f_{REF}}{V_{REF}} \cdot \Delta V_{TH}. \quad (9)$$

The output frequency also has an offset term, but its T.C. is independent of process variation because the capacitor ratio C_{S2}/C_{S1} is insensitive to process variation.

3. Simulation results

We confirmed the operation of our circuit with SPICE simulation using a set of 0.35-μm standard CMOS parameters and assuming a 3-V power supply. Reference voltage V_{REF} and clock f_{REF} were set to 0.75 V and 1 MHz using ideal voltage and clock sources. To study the dependence of output current I_{PTAT} and frequency f_{PTAT} on process variations, we performed Monte Carlo simulations assuming both within-die (WID) (intra-die) variation (e.g., $\sigma_{V_{TH}}$, σ_μ, $\sigma_{T_{OX}}$, σ_L, σ_W) and die-to-die (D2D) (inter-die) variation (e.g., ΔV_{TH}, $\Delta\mu$, ΔT_{OX}, ΔL, ΔW) in transistors and capacitors using the parameters provided by the manufacturer. For WID variation, we assumed that every parameter shows a Gaussian distribution that depends on device area (e.g., $\sigma_{V_{TH}} = A_{V_{TH}}/\sqrt{LW}$) [19–21]. For D2D variation, we assumed a uniform distribution (e.g., $-0.1\,\text{V} < \Delta V_{TH} < 0.1\,\text{V}$), which shows worst case corners independent of device area [19–21].

Fig. 5 shows the distribution of T.C. (f_{PTAT}) and T.C. (I_{PTAT}) in the temperature range from 10 to 80 °C, as obtained from Monte Carlo simulation of 100 runs. The T.C.s were normalized at the average value. Process sensitivities (σ/μ) of T.C. (f_{PTAT}) and T.C. (I_{PTAT}) were 2% and 6%, respectively. As discussed in Section 2.2, T.C. (I_{PTAT}) varied significantly with each run; this reflected the variation in capacitors for each run. In contrast, T.C. (f_{PTAT}) spread was small comparison with T.C. (I_{PTAT}), because T.C. (f_{PTAT}) was insensitive to capacitor variations. This way, process sensitivity (σ/μ) was improved to about 67% by converting current I_{PTAT} into frequency f_{PTAT}.

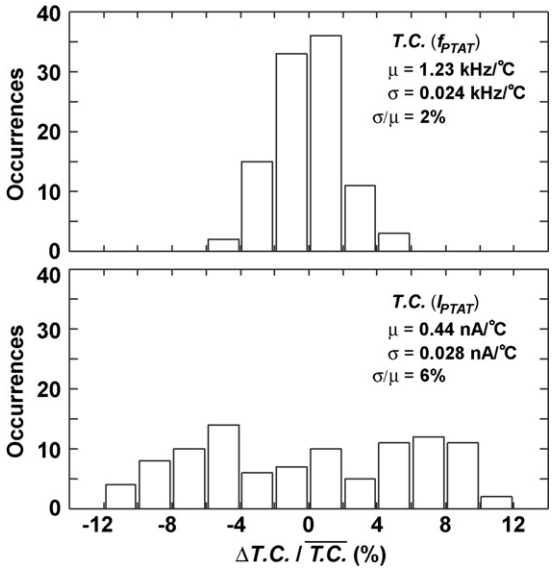

Fig. 5. Distribution of T.C. (f_{PTAT}) and T.C. (I_{PTAT}), as obtained from Monte Carlo simulation of 100 runs. Process sensitivity (σ/μ) of T.C. was improved to about 67% by converting current I_{PTAT} into frequency f_{PTAT}.

4. Experimental results

We fabricated a prototype chip using a 0.35-μm, 2-poly, 4-metal standard CMOS process. Fig. 6 shows a micrograph of this chip. The chip area is 0.08 mm^2 (= 230 × 360 μm) excluding I/O pads and the connections. The supply voltage was set to 3 V (the nominal voltage of lithium-ion batteries). Reference voltage V_{REF} of 0.75 V, and reference clock f_{REF} of 1 MHz were supplied from external sources (Semiconductor parameter analyzer and Wave form generator). To evaluate the tolerance to device-parameter variations of the circuit, we measured three samples on different chips from the same wafer.

Fig. 7 shows measured PTAT current as a function of temperature in a range from 10 to 80 °C. As expected from Eq. (4), the value of I_{PTAT} increased linearly with temperature. The values of T.C. from 0.49 to 0.56 nA/° C were observed in the three samples. Average T.C.

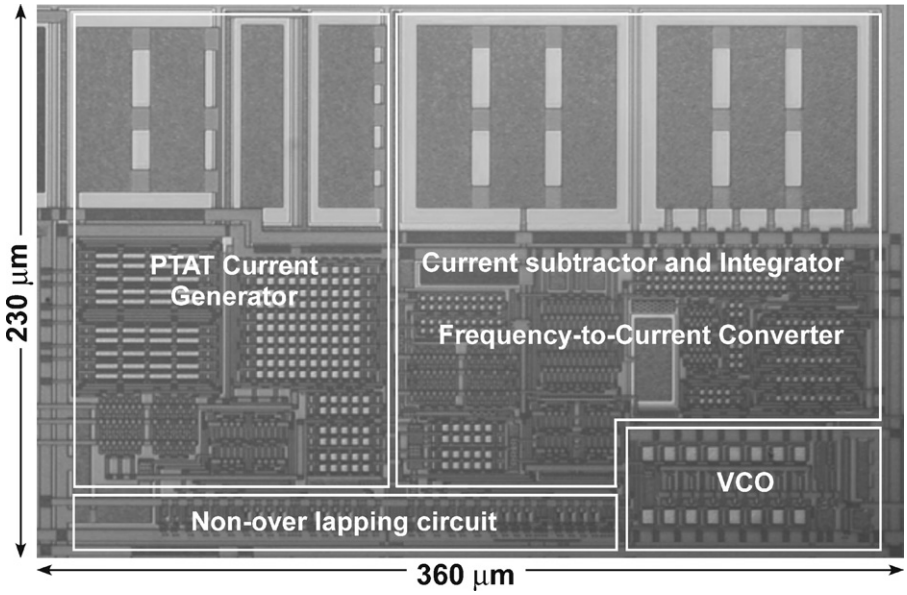

Fig. 6. Micrograph of prototype chip with area of 0.08 mm^2.

Table 1
Comparison of reported low-power CMOS temperature sensor circuits.

	This work	[8]	[9]	[11]	[12]	[13]
Sensor type	Subthreshold MOS. ΔV_{GS}	Bipolar Tr. ΔV_{BE}	Bipolar Tr. ΔV_{BE}	Delay line Temp-to-pulse	Strong. MOS. 4 Tr.	Subthreshold MOS. ΔV_{GS}
Process	0.35-μm, CMOS	2-μm, CMOS	0.7-μm, CMOS	0.35-μm, CMOS	90-nm, CMOS	0.18-μm, CMOS
Temp. range	10–80 °C	−40–120 °C	−55–125 °C	0–100 °C	50–125 °C	0-100 °C
V_{DD}	2.2–3 V	2.2–5 V	2.5–5.5 V	3–3.8 V	1 V	1.8 V
Conv. rate	100 samples/s [a]	2 samples/s	100 samples/s	2 samples/s	–	100 samples/s
Power	10 μW(@ 2.2 V) 27 μW(@ 3 V)	7 μW(@ 2.2 V)	62.5 μW(@ 2.5 V) 137.5 μW(@ 5.5 V)	10 μW(@ 3.3 V)	25 μW(@ 1 V) (only analog)	0.22 μW(@ 1.8 V)
	Room temp.	N.A.	N.A.	N.A.	N.A.	Room temp.
Inaccuracy	−1.8/+1 °C	±1 °C	±0.1 ° C (3σ)	−0.7/+0.9 °C	−1/+0.8 °C	−1.6/+3 °C
Calibration	1-point	2-points	1-point	2-points	2-points	2-points
Chip area	0.08 mm^2	1.5 mm^2	4.5 mm^2	0.175 mm^2	48 μm^2 (only analog)	0.05 mm^2

[a] Temperature resolution: 0.1 °C.

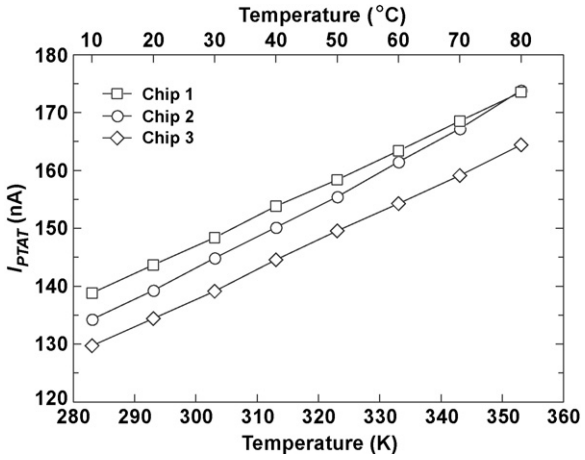

Fig. 7. Measured PTAT current I_{PTAT} as a function of temperature. Average T.C. is 0.5 nA/°C.

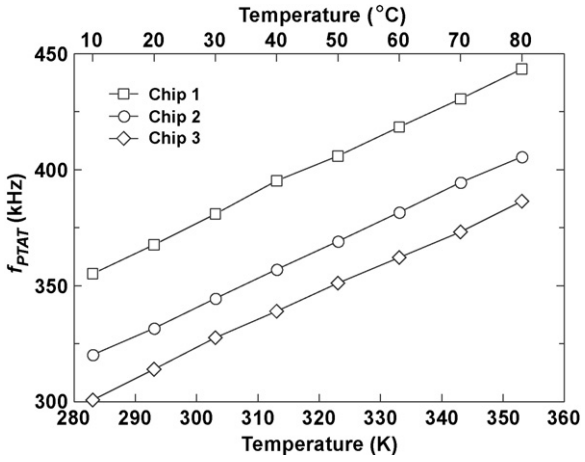

Fig. 8. Measured output frequency f_{PTAT} as a function of temperature. Average T.C. is 1.2 kHz/°C.

was 0.5 nA/°C. However, the measured values of I_{PTAT} had small offset currents and T.C. variations that depended on individual chips. These are caused by the threshold voltage mismatch of the transistor pair (M_1 and M_2) and capacitance variation in the PTAT current generator as discussed in Section 2.2. The T.C. variations of the results can be canceled, as discussed later.

Fig. 8 shows output frequency f_{PTAT} as a function of temperature. The value of f_{PTAT} increased linearly with temperature, as expected from Eq. (7). The values of T.C. from 1.18 to 1.25 kHz/° C were observed in the three samples, and average T.C. was 1.2 kHz/°C.

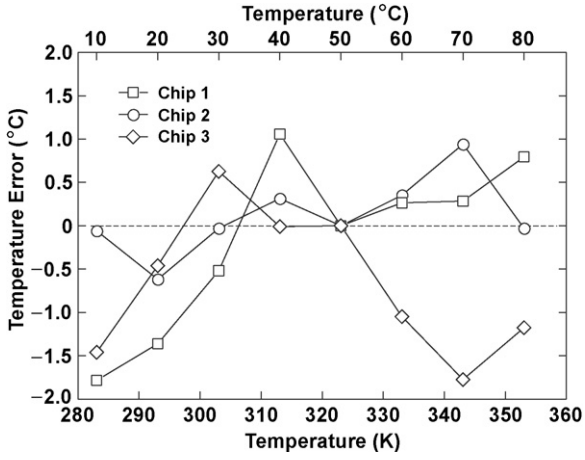

Fig. 9. Calculated temperature error after one-point calibration at 50 °C. Temperature error is within −1.8 to +1 °C.

Although the output frequencies have a small offset, its T.C. is almost the same for every chip. In this measurement, the T.C. of the PTAT currents changes by ±7% with process variations, while the T.C. of the output frequency changes by only ±3%. This is so because the variation of the T.C. in the PTAT current that is dependent on the capacitor variation can be canceled by converting the output frequency independent of the capacitor variation as discussed in Section 2.2. Therefore, the T.C. of the output frequency is almost independent of process variations.

To reduce the offset error of the output frequency, we performed one-point calibration so that the offset between the theoretical results and the measurement results at 50 ° C would be eliminated. This calibration made it possible to determine temperature from the value of f_{PTAT} within a small error of −1.8 to +1 ° C as plotted in Fig. 9. Because the T.C. variations of the output frequency can be canceled, as described above, the one-point calibration will enable us to compensate for the offset with process variation.

Table 1 summarizes the characteristics of our sensor in comparison with other low-power CMOS temperature sensors reported in [8–13]. The power dissipation was 10 μW at a 2.2-V supply voltage and a conversion rate of 100 samples/s. The line regulation was 0.8%/V in a supply voltage range from 2.2 to 3 V. It is clear from the table that the sensor is comparable to other circuits in terms of power dissipation. In regard to reported circuits [5–14], there are trade-offs between power dissipation and temperature inaccuracy after calibration. Our sensor used only one-point calibration, and its inaccuracy was within −1.8 to +1 °C. Therefore, our sensor device was able to achieve an appropriate trade-off between power dissipation and temperature inaccuracy after calibration.

5. Conclusion

We developed an ultra-low-power temperature sensor device consisting of subthreshold MOSFET circuits. The device used a PTAT current generator controlled with an external reference clock and a frequency-locked loop biased with an external reference voltage, and it generated a PTAT clock frequency. We made a prototype chip, using a 0.35-μm CMOS process, and demonstrated its operation by measurements. The output frequency of our sensor circuit was insensitive to process variation, so the circuit used only one-point calibration. The accuracy of the sensor output was within −1.8 to +1 °C in a temperature range from 10 to 80 °C. The power dissipation was about 10 μW. Our sensor would be suitable for use in subthreshold-operated, power-aware LSIs such as RFIDs, implantable medical devices, and smart sensor-network nodes.

Acknowledgments

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