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On-Chip Fixed-Pattern-Noise Canceling with Non-Destructive Intermediate Readout Circuitry for CMOS Active-Pixel Image Sensors

Ryo Kagaya, Masayuki Ikebe, Tetsuya Asai, and Yoshihito Amemiya

Department of Electrical Engineering, Hokkaido University,
Kita 13, Nishi 8, Kita-ku, Sapporo, 060-8628 Japan
E-mail: kagaya@sapiens-ei.eng.hokudai.ac.jp

Abstract

We propose a new method of canceling the fixed-pattern noise of CMOS active-pixel image sensors caused by the threshold mismatch of MOS FETs in pixel circuits. This method uses with non-destructive intermediate readout circuitry. Assuming a TSMC 0.25-μm mixed-signal process, we designed a CMOS image sensor in which the canceling circuit was implemented for each column of the pixel-sensor array. Simulation results revealed that threshold mismatch of $O(10^{-1})$ V could be reduced to $O(10^{-4})$ V within a settling time of $O(10^{-7})$ s.

Keywords: CMOS image sensor, fixed-pattern-noise, noise canceling

1 Introduction

Ordinary three-transistor pixel circuits in CMOS active-pixel image sensors have no capability to cancel fixed-pattern noise (FPN). Since this noise is a serious problem in CMOS image sensors, recent sensors have suppressed FPN by using analog-signal-processing circuits such as correlated double sampling (CDS) circuits that are put on the periphery of the pixel array. However, the CDS is inherently a destructive readout operation, and this disables us from reading out intermediate image signals. To overcome this problem, we propose a new circuity for canceling FPN with non-destructive intermediate readout, which can be applied to various image-processing applications [1].

2 Pixel Circuit with Adaptive Initializing Circuitry

Our method of FPN canceling that permits intermediate readout is based on *pixel-level adaptation to the threshold voltage of a MOS FET* in each pixel circuit. Figure 1 shows an active pixel circuit (gray box) with the FPN canceling circuit we propose. The canceling circuit consists of a current source (M4) and a operational transconductance amplifier (OTA) and forms a feedback loop with the pixel circuit. With this canceling circuit, we can compensate for mismatch of M2 between pixels (this mismatch causes FPN). The operating cycle of the pixel circuit is the same as conventional active pixels; that is, initializing, charging, and analog-to-digital conversion (ADC). During the initializing period,

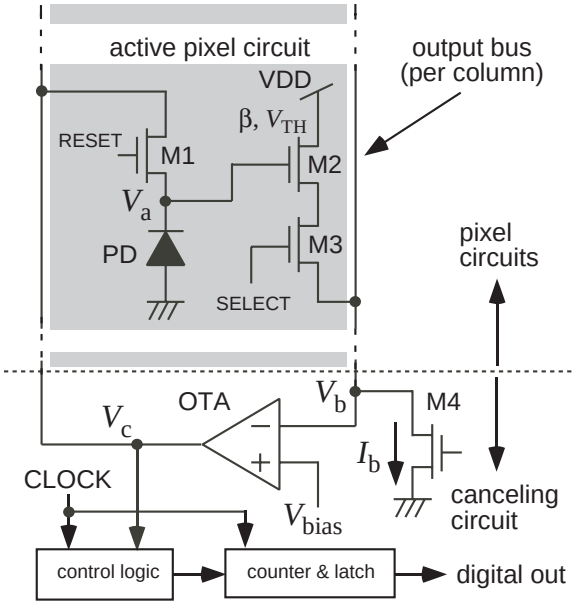

Fig. 1. Adaptive pixel circuit with ADC circuitry

M1 and M3 are turned on. The output of the OTA is

$$V_{\rm c} = \frac{A}{A+1}\left(V_{\rm bias} + V_{\rm TH} + \sqrt{\frac{I_b}{\beta}}\right), \qquad (1)$$

where A represents the gain of the OTA, $V_{\rm bias}$ the bias voltage for the non-inverting terminal, $V_{\rm TH}$ the threshold voltage of M2, β the transconductance of M2, and I_b the drain-source current in M4. Assuming that A is far larger than 1 and M4 is saturated, we obtain that $V_{\rm a} = V_{\rm c} \approx V_{\rm bias} + V_{\rm TH} + \sqrt{I_b/\beta}$. This shows that the pixel can be adapted to produce a voltage of $V_{\rm bias}$ on the output bus ($V_{\rm b}$) independently of $V_{\rm TH}$ and β of M2 and I_b in M4.

After the initializing period, transistors M1 and M3 are turned off, and each pixel is exposed to input photosignals (charging period). Then, transistor M3 is turned on in the ADC period and the pixel is connected to the output terminal bus. By applying a ramp voltage to the $V_{\rm bias}$ terminal, the OTA combined with additional control logic and counter circuits performs single-slope ADC. Unlike CDS, the pixel output can successively be read out without initialization, and this enables us to read out intermediate images.

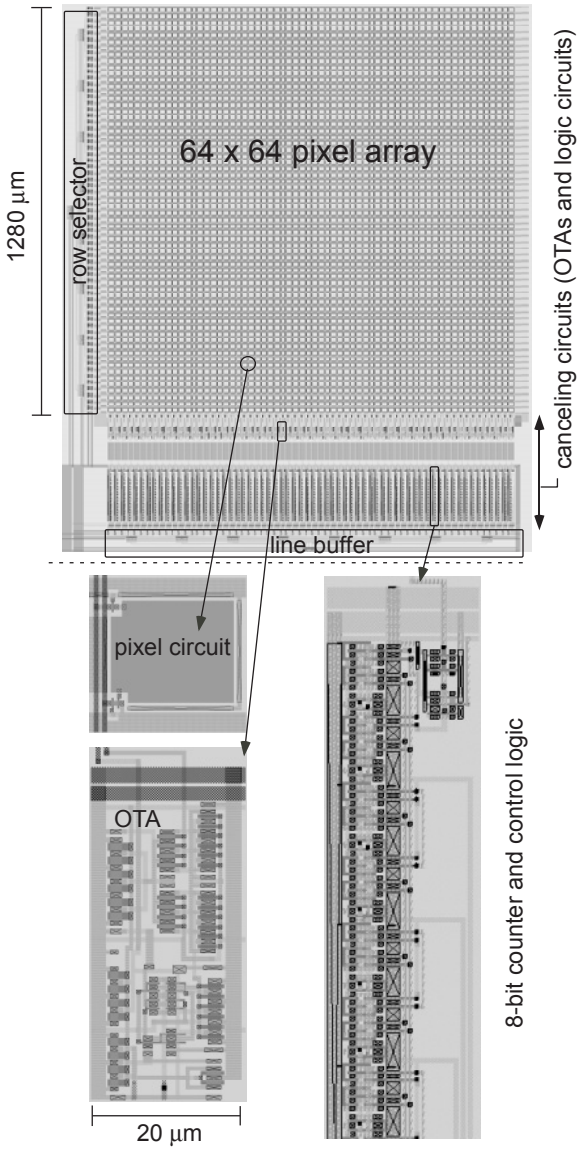

Fig. 2. Device layout consisting of 64 × 64 pixel circuits.

3 Device Layout and Simulation Results

We designed a CMOS image sensor using the proposed circuit with TSMC's 0.25-μm mixed-signal scalable CMOS rule. Figure 2 has the device layout consisting of 64 × 64 pixel circuits and 64 canceling circuits. The canceling circuit was put on the bottom of the layout.

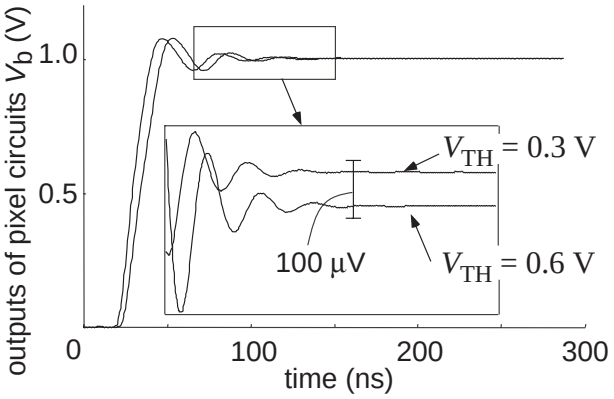

Fig. 3. Simulation results for FPN operation

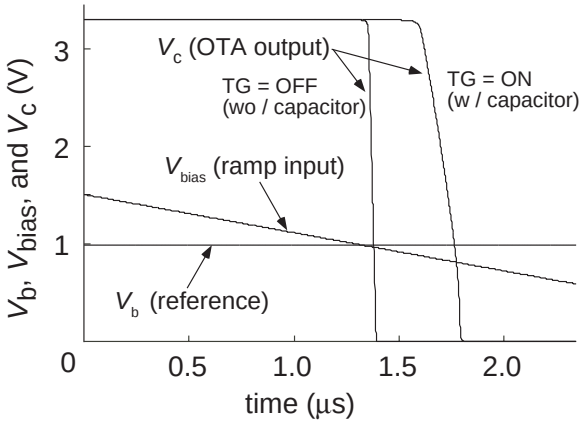

Fig. 4. Simulation results for ADC operation

Figure 3 plots the simulation results for FPN operation (VDD = 3.3 V, $V_{\rm bias}$ = 1.0 V, I_b = 1 μA), with the threshold voltage of M2 as a parameter. In this example, the output voltage of a pixel was initially set to 0 V at time = 0. For two M2 threshold voltages, 0.3 V and 0.6 V, output voltage $V_{\rm b}$ converged to 1 V within a minute difference of 100 μV. The settling time was 100 ns.

The OTA plays a dual role in our circuitry; i.e., threshold compensation and ADC. To achieve a stable unity gain operation (initializing period) and a high slew-rate operation (ADC period), we implemented *selective phase-compensation* by using a capacitor controled by a transfer gate (TG) connected in series with the capacitor. During the initializing period, the TG is turned on and the capacitor compensates the OTA for unity-gain operation, while the TG is turned off during the ADC period and the OTA operates as a high slew-rate comparator. Figure 4 plots the result of operation during the ADC period (VDD = 3.3 V, $V_{\rm b}$ = 1.0 V). The ADC resolution in our OTAs with the selective phase-compensation capacitor was 8 bits at 0.3 MHz.

4 Concluding Remarks

- We proposed new on-chip fixed-pattern-noise canceling circuit for CMOS active-pixel image sensors.
- This circuit enables us to read out intermediate image data non distructively.
- When $V_{\rm bias}$ = 1.0 V and VDD = 3.3 V, the variation between pixels improved from $O(10^{-1})$ V to $O(10^{-4})$ V. The corresponding resolution of depth was 18 bits.
- The settling time was $O(10^{-7})$ s ($\ll$ 33 ms @ 30 FPS; focal-plane shutter) when $I_{\rm b}$ = 1 μA.
- ADC resolution, using a selective phase compensation, was 8 bits at 0.3 MHz, even though an ordinary OTA circuit was used.

5 References

[1] D. Handoko, S. Kawahito, Y. Tadokoro, and A. Matsuzawa "A CMOS image sensor with non-destructive intermediate readout mode, for adaptive iterative search motion vector estimation" *IEEE Workshop CCD and Advanced Image Sensors*, pp. 52–55, June 2001.