PAPER Special Section on Analog Circuits and Related SoC Integration Technologies

An On-Chip PVT Compensation Technique with Current Monitoring Circuit for Low-Voltage CMOS Digital LSIs

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SUMMARY An on-chip process, supply voltage, and temperature (PVT) compensation technique for low-voltage CMOS digital circuits was proposed. Because the degradation of circuit performance originates from the variation of the saturation current in transistors, we developed a compensation circuit consisting of a reference current that is independent of PVT variations. The circuit is operated so that the saturation current in digital circuits is equal to the reference current. The operations of the circuit were confirmed by SPICE simulation with a set of 0.35-μm standard CMOS parameters. Monte Carlo simulations showed that the proposed technique effectively improves circuit performance by 71%. The circuit is useful for on-chip compensation to mitigate the degradation of circuit performance with PVT variation in low-voltage digital circuits.

key words: *digital circuits, threshold voltage variation, compensation circuit, PVT variation*

1. Introduction

The power dissipation in LSIs is an important matter in battery-powered electronic devices such as cellular phones, laptops, and portable gadgets because these devices have to operate for a long lifetime with limited energy sources. Various techniques for low-power digital circuits have been investigated [1]. Among such techniques, reduction of power supply voltage V_{DD} is the most effective and direct way because power dissipation has a quadratic dependence on supply voltage. Moreover, with recent progress in device technology, the high V_{th} MOSFET–which can further reduce power dissipation with reducing a leakage current–has become available. However, when the values of supply voltage V_{DD} and threshold voltage V_{th} of MOSFETs come close, the variation of threshold voltage has a significant impact on circuit performance. This is because the saturation current of a MOSFET depends on both supply voltage V_{DD} and threshold voltage V_{th}, and the variation of the current is proportional to the expression of $\alpha/(V_{DD} - V_{th})$, where α is a carrier mobility degradation factor [2], [3]. Both low supply voltage operation and the use of high V_{th} MOSFET therefore tend to increase variation in circuit performance.

The variation of threshold voltage in a MOSFET is due to process and temperature variations, namely, about ±0.1 V in a worst process variation and 0.1 V in a temperature range of −20 to 100°C. The variation degrades circuit performance; accordingly, LSI designers should pay close attention to the variations. Several compensation techniques have been reported [4]–[8]. In [4] and [5], a reference clock was used to compensate for the variations, and in [6]–[8], a substrate biasing or supply voltage control, or both, were used. However, these techniques involve the use of several circuit blocks and thus result in a complex and large-scale circuit configuration.

To solve these problems, we developed an on-chip process, supply voltage, and temperature (PVT) compensation technique by using a variation-tolerant reference current for low-voltage CMOS digital circuits. Because the degradation in performance of the circuit comes from the variation of saturation current due to variation of threshold voltage under low-voltage operation, a compensation technique using a reference current that is independent of PVT variations was developed [9]. The circuit has a compact configuration and is useful for low-voltage CMOS digital LSI systems. In the following, Sect. 2 describes the effect of the process and temperature variations on digital circuit performances. Section 3 shows the compensation architecture and the configuration of the compensation circuit we propose. Section 4 demonstrates the operation of the proposed circuit with simulation results for various variations. Note that, all the simulations in this work were performed using a SPICE, SPECTRE-level 53 model, and the parameter set of a 0.35-μm 2P4M-standard CMOS process.

2. Effect of Process and Temperature Variations on Digital Circuit Performances

The process variations cause degradation of circuit performance and low fabrication yield in low-voltage circuits. In CMOS process parameters, variation of threshold voltage of a MOSFET is one of the serious problems because threshold voltage has a significant impact on its drain current.

The variation of threshold voltage can be classified broadly into two categories [10], [11]: within-die (WID), or intra-die, variation and die-to-die (D2D), or inter-die, variation. The former affects the relative accuracy of transistors placed closely within a chip and depends on the transistor sizes [12]. The latter affects the absolute accuracy of the chip and degrades the performance between chips. Because digital circuits consist of minimum-sized transistors, the performance of digital circuits is affected by both WID and D2D variations. However, according to the central limit

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theorem, the effect of WID variations is statistically averaged out to the value defined by the D2D variations [11]. Because the critical path of digital circuits consists of a cascade chain comprising a number of basic gates, the effect of WID variations will be small. However, the D2D variations cannot be ignored.

In the present study, to evaluate the effects of process and temperature variations in digital circuits, a delay variation of a CMOS inverter chain was analyzed. We performed Monte Carlo simulations assuming both D2D variation (e.g., $\delta V_{th}, \delta\mu, \delta T_{ox}, \delta L, \delta W$) and WID variation (e.g., $\sigma_{V_{th}}, \sigma_{\mu}, \sigma_{T_{ox}}, \sigma_L, \sigma_W$) in transistor parameters. For D2D variation, we assumed a uniform distribution (e.g., $-0.1\,\text{V} < \delta V_{th} < 0.1\,\text{V}$), which shows worst case corners independent of device area [10]–[12]. For WID variation, we assumed that every parameter shows a Gaussian distribution that depends on device area (e.g., $\sigma_{V_{th}} = A_{V_{th}}/\sqrt{LW}$) [11], [12].

2.1 Delay Analysis of Digital Circuits

The delay τ of an inverter can be expressed by

$$\tau = \frac{C_{load} V_{DD}}{I_{on}}, \tag{1}$$

where C_{load} is load capacitance, V_{DD} is supply voltage, and I_{on} is saturation current. Saturation current I_{on} is given by

$$I_{on} \sim \frac{W}{L}\mu C_{ox}(V_{DD} - V_{th})^{\alpha}, \tag{2}$$

where L is channel length, W is channel width, μ is carrier mobility, C_{ox} is gate oxide capacitance, and α is a carrier mobility degradation factor [3]. Load capacitance C_{load} can be approximated by the gate capacitance of the next inverter stage and is given by

$$C_{load} \sim C_{ox} LW. \tag{3}$$

Therefore, from Eqs. (1), (2), and (3), the delay τ as shown in Eq. (1) can be rewritten as

$$\tau \sim \frac{L^2 V_{DD}}{\mu (V_{DD} - V_{th})^{\alpha}}. \tag{4}$$

Note that the delay τ is independent of the channel width W. Under the assumption that each parameter in Eq. (4) varies $\pm\delta$ from the typical value, the delay variation $\delta\tau/\tau$ is expressed as

$$\begin{aligned} \frac{\delta\tau}{\tau} &= \frac{1}{\tau}\left(\frac{\partial\tau}{\partial L}\delta L + \frac{\partial\tau}{\partial\mu}\delta\mu + \frac{\partial\tau}{\partial V_{th}}\delta V_{th}\right) \\ &= 2\frac{\delta L}{L} + \frac{\delta\mu}{\mu} + \frac{\alpha}{V_{DD} - V_{th}}\delta V_{th}. \end{aligned} \tag{5}$$

Delay variation $\delta\tau/\tau$ depends on the terms of channel length variation $\delta L/L$, carrier mobility variation $\delta\mu/\mu$, and threshold voltage variation $\delta V_{th}/(V_{DD} - V_{th})$, which depends on supply voltage. In general, the degradation in performance of a digital circuit is dominated by the channel length variation. In low-voltage digital circuits, however, threshold voltage variation becomes a key factor in the delay variation $\delta\tau/\tau$ instead of the channel length variation.

Table 1 Standard value (typical), its variability value (δ) and its degree of variability (δ/typical or $\delta/(V_{DD}$-typical)) of each parameters with a set of 0.35-μm standard CMOS parameter we used.

parameter	typical	δ	$\delta/(V_{DD}$–typical) (%) V_{DD}=2 V	$\delta/(V_{DD}$–typical) (%) V_{DD}=1 V
V_{thn} (V)	0.52	±0.1	6.8	20.9
V_{thp} (V)	0.72	±0.1	7.8	35.8
			δ/typical (%)	
L (μm)	0.35	±0.05	14.3	
W (μm)	0.4	±0.075	18.8	
μ_n (cm^2/V·s)	370	±16.5	4.5	
μ_p (cm^2/V·s)	126	±13.5	10.7	

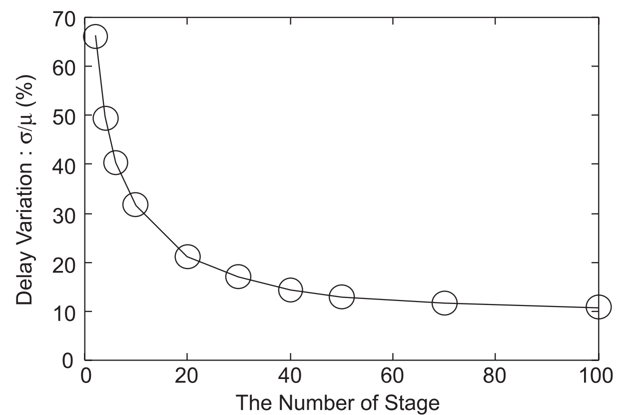

Fig. 1 Delay variation of an inverter chain circuit as a function of the number of inverter stages from 100-runs Monte Carlo simulations assuming WID variations. Supply voltage: 1 V.

Table 1 shows examples of device parameter values (threshold voltage V_{th}, channel length L, channel width W, and carrier mobility μ) provided by the manufacture; standard value (typical), its variability value (δ) and its degree of variability (δ/typical or $\delta/(V_{DD}$-typical)) of each parameters with a set of 0.35-μm standard CMOS parameter we used. Because the threshold voltage of a pMOSFET (0.72 V) is 1.4 times larger than that of an nMOSFET (0.52 V) in the process, the variation of threshold voltage of the pMOSFET has a significant impact on circuit performance than that of nMOSFET.

2.2 Impact of WID Variations

To study the effect of WID variation on circuit performance, an inverter chain circuit was analyzed by Monte Carlo simulation considering WID variations. Because the delay has a Gaussian distribution (σ: standard deviation, μ: average), the coefficient of variation (σ/μ) of the delay per inverter stage was evaluated. Figure 1 plots the coefficient of variation in delay time as a function of the number of inverter

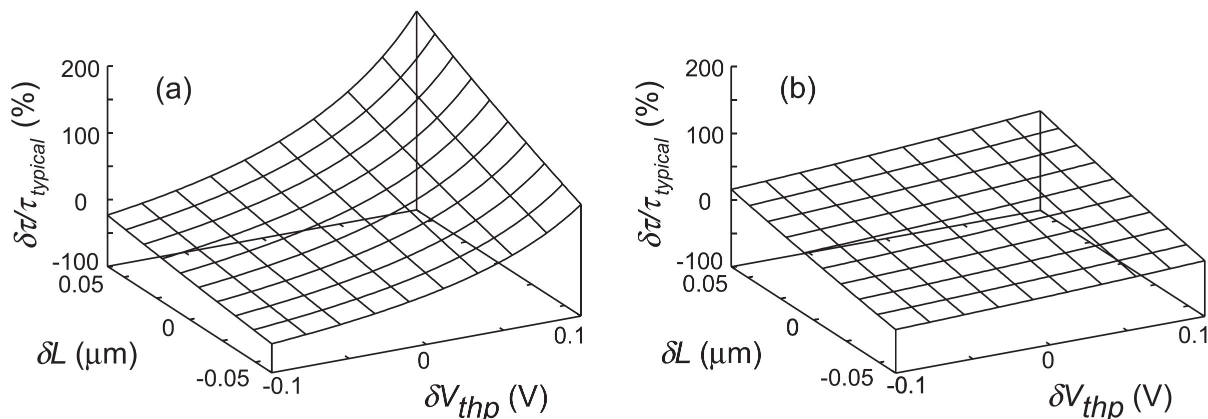

Fig. 2 Calculated delay variation of an inverter chain circuit as a function of pMOSFET threshold voltage variation δV_{thp} and channel length variation δL. (a) Supply voltage: 1 V; (b) supply voltage: 2 V.

stages. Clearly, (σ/μ) decreases as the number of inverter stages increases. This is because WID variations of an inverter are averaged as the number of inverter stages increases. In most digital circuits, the number of stages is high enough, so the effect of WID variations is small enough compared to the D2D variations. For example, the critical path of 16- and 32-bit carry-look-ahead adders consist of 48- and 96-stages, and 16- and 32-bit pipelined multipliers consist of 81- and 161-stages.

2.3 Impact of D2D Variations

To verify the effect of the D2D process variations at low- and high-supply-voltages, Eq. (5) was evaluated numerically with parameters for a 0.35-μm CMOS. Because the threshold voltage of a pMOSFET is 1.4 times larger than that of an nMOSFET in the process as shown in Table 1, the variation of threshold voltage of the pMOSFET has a significant impact on circuit performance. Figure 2 plots the calculated delay variation $(\delta\tau/\tau)$ of an inverter chain circuit as a function of D2D pMOSFET threshold voltage variation δV_{thp} and D2D channel length variation δL. For a supply voltage of 2 V (Fig. 2(b)), the impacts of pMOSFET threshold voltage variation and channel length variation are comparable. However, at a lower voltage of 1 V (Fig. 2(a)), the delay variation with pMOSFET threshold voltage variation δV_{thp} increases drastically.

The delay variations of the circuit were analyzed by SPICE simulation with Monte Carlo analysis assuming D2D variations. Figure 3 shows the simulated delay variation of an inverter chain circuit as a function of supply voltage. The results in the case in which parameters (V_{thn}, V_{thp}, L, W, μ_n and μ_p) were varied individually are also plotted to separate the effects of each parameter on the delay variation. At higher supply voltage ($V_{DD} > 1.2$ V), the delay variation was dominated by the channel length variation. On the other hand, at lower voltage ($V_{DD} < 1.2$ V), the effect of the pMOSFET threshold voltage variation became worse than that of channel length variation and became a key factor in the delay variation. The variations in the mobility and the channel width are small enough compared to that of the threshold voltage and the channel length variations at a wide range of supply voltages. Therefore, the variation of threshold voltage has a significant impact on digital circuit performances at a low-voltage operation.

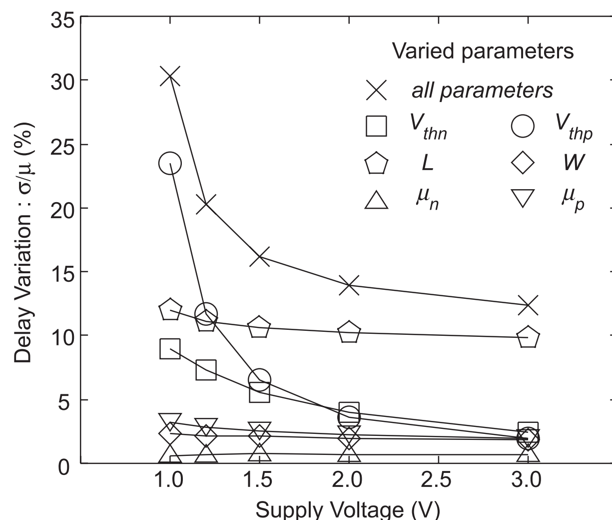

Fig. 3 Delay variation of inverter chain circuit as a function of the supply voltage from 100-runs Monte Carlo simulations assuming D2D variations. The results that parameters varied individually are also plotted.

2.4 Temperature Variation

Temperature variation also causes performance degradation in CMOS digital LSIs because parameters such as threshold voltage V_{th} and mobility μ depend on temperature. In this section, the temperature dependence of the low-voltage digital circuit is discussed.

The temperature dependence of threshold voltage V_{th} and mobility μ is given by

$$\mu = \mu_0 \left(\frac{T_0 + \delta T}{T_0} \right)^{-m}, \tag{6}$$

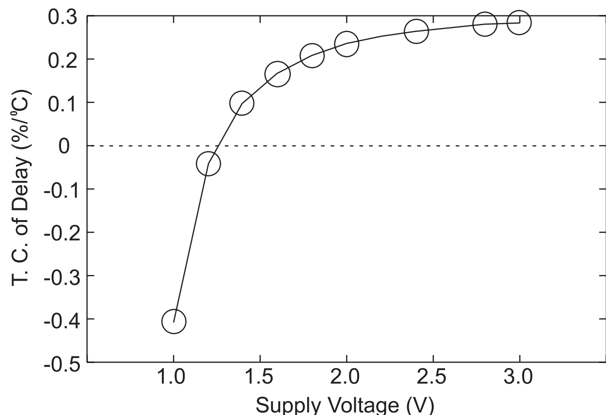

Fig. 4 Simulated normalized temperature coefficient of inverter chain delay as a function of supply voltage.

$$V_{th} = V_{th0} - \kappa(T_0 + \delta T), \tag{7}$$

where μ_0 is carrier mobility at room temperature, m is the mobility temperature exponent, T_0 is room temperature, δT is the temperature change from T_0, V_{th0} is the threshold voltage at absolute zero temperature, and κ is the temperature coefficient of the threshold voltage [13].

The delay variation $\delta\tau/\tau$ in Eq. (4) with temperature is given by

$$\begin{aligned}\frac{\delta\tau}{\tau} &= \frac{1}{\tau}\left(\frac{\partial\tau}{\partial T}\delta T\right)\\ &= \frac{1}{\tau}\left(\frac{\partial\tau}{\partial\mu}\frac{\partial\mu}{\partial T}\delta T + \frac{\partial\tau}{\partial V_{th}}\frac{\partial V_{th}}{\partial T}\delta T\right)\\ &= \left(\frac{m}{T_0} - \frac{\alpha\kappa}{V_{DD} - V_{th0} + \kappa T_0}\right)\delta T.\end{aligned} \tag{8}$$

As with the process variation discussed in the previous section, the variation of delay with temperature depends on supply voltage, as shown in the second term of Eq. (8).

Figure 4 shows the simulated temperature coefficient of the delay in an inverter chain circuit as a function of supply voltage. The temperature coefficient is derived from the simulated delay time. In the figure, positive (or negative) values mean a delay increase (or decrease) with temperature. At a higher supply voltage, temperature coefficient of the delay is positive. This is because on-current of MOSFET decreases with temperature due to mobility degradation and delay time increases with temperature. As shown in Eq. (8), the second term, which depends on both supply voltage and threshold voltage, has much less temperature dependence on the delay variation at the higher voltage region compared to the first term in Eq. (8). It is thus concluded that the temperature dependence of carrier mobility is a key factor in the variation of delay at a higher voltage. However, at lower voltage, the temperature coefficient gradually decreases with decreasing supply voltage as a result of the second term in Eq. (8). At a supply voltage of 1.1 V, the temperature coefficient of the delay becomes zero. This result means that the first and second terms in Eq. (8) became comparable at the supply voltage. At a supply voltage below 1.1 V, the temperature coefficient becomes negative, and the second term in Eq. (8) becomes a key factor in the variation of delay.

3. Compensation Technique with Monitoring the On-Current Variations

As explained in the previous sections, the delay variation of the circuit depends on both supply voltage V_{DD} and threshold voltage V_{th} when the circuit operates at low supply voltage. Operating the circuit at low supply voltage while sufficient performance is maintained, a PVT compensation technique is required. Because the critical path of digital circuits consists of a cascade chain comprising several basic gates, the effect of WID variations will be small. However, the D2D variations cannot be ignored. Therefore, our circuit compensates for the D2D process variations in digital circuit performances. Accordingly, as explained in this section, we derived an on-chip process compensation technique for low-voltage digital circuits. The technique uses a reference current that is tolerant to PVT variations.

Figure 5 shows the entire compensation circuit. The circuit consists of a current monitoring circuit which has a current reference circuit and replica transistors, a switching DC/DC converter, a buffer circuit and a CMOS digital circuit. In this compensation, supply voltage and body-bias voltage in the digital circuits are controlled so that the on-current of the digital circuits is equal to the reference current. Because reference current is tolerant to PVT variations, delay variation of the digital circuit can be compensated. The details of the circuit operation are as follows.

3.1 Current Reference Circuit

The developed compensation technique uses a reference current I_{ref} that is independent of PVT variations. The reference current I_{ref} is generated by a threshold voltage monitoring circuit [14], a non-inverting amplifier, and an output transistor M_{n0}. (The circuit configuration is shown on the left hand side of Fig. 5.) The threshold voltage monitoring circuit generates a voltage V_{th0n} that is based on the threshold voltage of a MOSFET at absolute zero temperature [14]. Output voltage V_{th0n} has linear dependence on D2D threshold voltage variation. Therefore, by making use of the voltage as a bias voltage for a transistor, a reference current that is independent of threshold voltage variation can be obtained because the output voltage monitors the threshold voltage in an LSI chip. However, although the variation of threshold voltage can be canceled by the monitoring circuit, temperature dependence on the mobility still exists. To compensate for the temperature dependence of the current, a non-inverting amplifier is used to cancel the temperature dependence of the mobility. The amplifier accepts and amplifies voltage V_{th0n} to a higher voltage, V_{bias}, by setting the appropriate ratio of resistors so that the temperature coefficient of the current becomes zero. Transistor M_{n0} accepts the voltage V_{bias} and generates a process and temperature

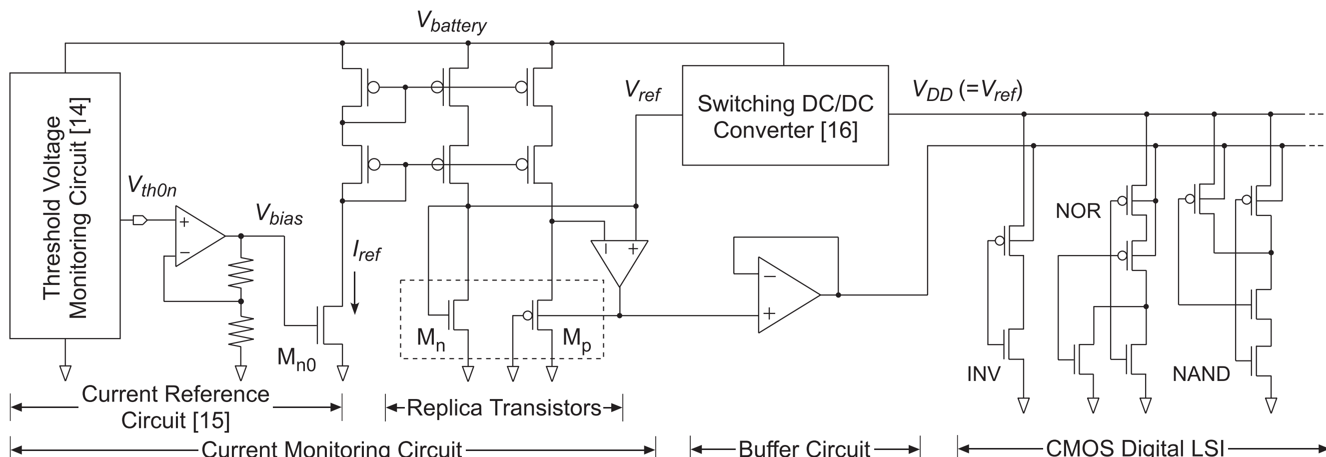

Fig. 5 Schematic of proposed compensation circuit.

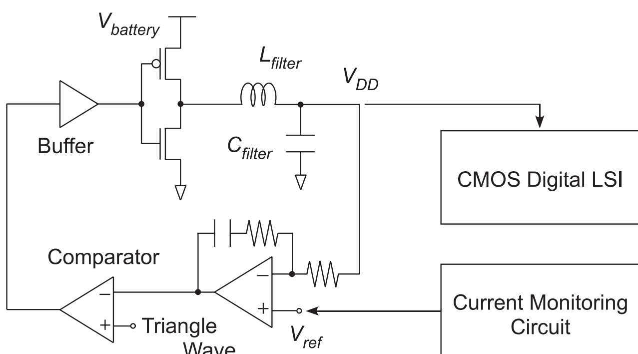

Fig. 6 Schematic of switching DC/DC converter based on PWM control [16].

compensated reference current I_{ref}. In this way, a reference current that is tolerant to PVT variations can be obtained. The details of the current reference circuit are presented in [15].

3.2 Compensation Circuit

To generate appropriate supply voltage and body-bias voltage, a current monitoring circuit and a buffer circuit are used in our compensation. Transistors M_n and M_p are the replica transistors of a digital circuit for monitoring and controlling the process and the temperature variation. These transistors consist of series-connected transistors and generate an appropriate voltage V_{ref}, that is used as a reference voltage for a switching DC/DC converter.

The diode-connected transistor M_n accepts I_{ref} through a pMOS current mirror and generates gate-source voltage V_{ref}, which is used as supply voltage V_{DD} for a digital circuit through the switching DC/DC converter shown in Fig. 6 [16]. The switching DC/DC converter can step down battery voltage to supply voltage of digital circuit with high-efficiency and high-driving. The circuit operates with PWM (pulse-width-modulation) control and PI (proportional-integral) feedback operation [16]. Because the supply voltage of nMOSFETs in digital circuits is the same as the replica transistor M_n, the saturation current of nMOSFETs in digital circuits is controlled so as to be the same current with the reference current I_{ref}. To control the saturation current of the pMOSFET, a diode-connected transistor M_p, and operational amplifier are used. The operational amplifier monitors the gate-source voltages of transistors M_n and M_p through the bulk terminal of transistor M_p. The operational amplifier controls the voltage of the bulk terminal of transistor M_p so that the current of pMOSFET in digital circuits is equal to the reference current I_{ref}. The buffer circuit accepts the generated bulk voltage and applies it to the bulk terminals of the pMOSFETs in digital circuits in order to control the saturation current in the pMOSFETs. This way the saturation current in both the nMOSFETs and pMOSFETs in the digital circuits are kept to reference current I_{ref}. Because reference current I_{ref} is independent from D2D process and temperature variation, PVT variations of the digital circuits can be compensated.

4. Simulation Results

The operations of the circuit were confirmed by Monte Carlo simulations assuming both D2D and WID variations. Voltage $V_{battery}$ was set to 3.3 V (under the assumption that a lithium-ion rechargeable battery is used). The delay variation of 8-bit carry-look-ahead adder was studied by setting supply voltage V_{DD} at 1 V.

Figure 7 shows the delay variation (σ/μ) as a function of the supply voltage. Although the delay variation without the compensation circuit increased at low voltage operation, the delay variations with compensation were able to be drastically suppressed at a supply voltage below 1.2 V. Figure 8 shows the distribution of the propagation delay variation of the circuit. The process sensitivities (σ/μ) in the case with and without the compensation technique were 10.3% and 36.1%, respectively, and can be improved to about 71% by using the proposed compensation technique. Figure 9 shows the simulated propagation delay of a critical path of 8-bit

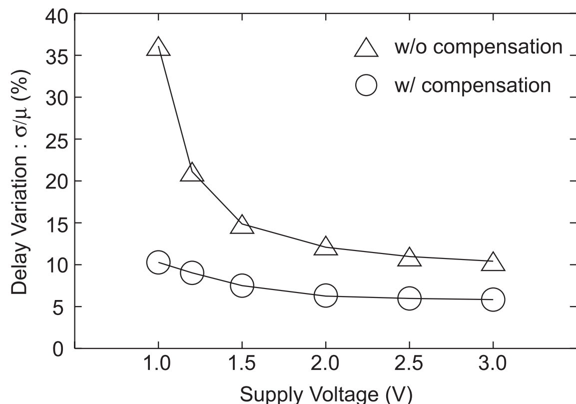

Fig. 7 Delay variation in a critical path of 8-bit carry-look-ahead adder with/without our compensation circuit as a function of the supply voltage from 200-runs Monte Carlo simulations assuming both D2D and WID variations.

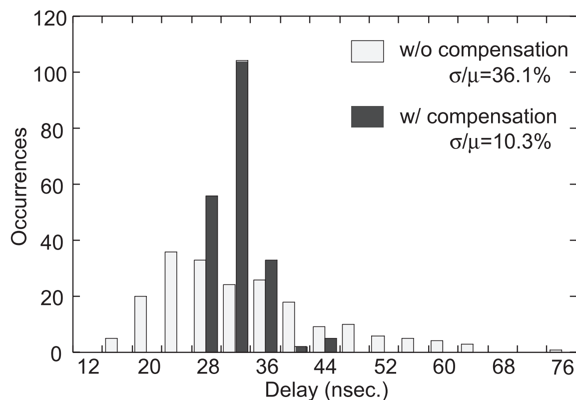

Fig. 8 Distribution of propagation delay in a critical path of 8-bit carry-look-ahead adder with/without our compensation circuit calculated from 200-runs Monte Carlo simulations assuming both D2D and WID variations.

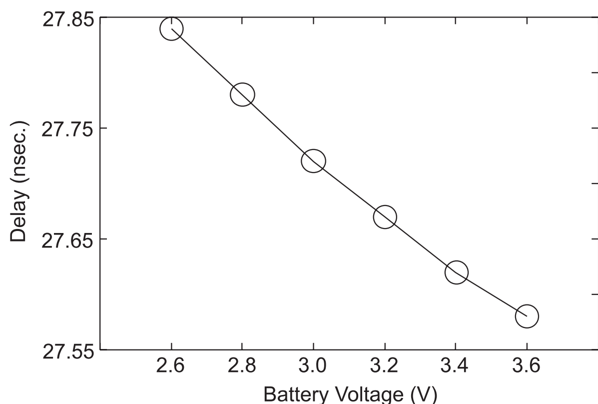

Fig. 9 Simulated propagation delay in critical path of 8-bit carry-look-ahead adder as a function of power supply $V_{battery}$ with compensation circuit. Line regulation was 0.9%/V.

carry-look-ahead adder with the compensation circuit as a function of voltage $V_{battery}$. The line regulation of the propagation delay is 0.9%/V. Figure 10 shows the simulated delay as a function of temperature from −20 to 80°C. In the with-compensation case, delay is almost constant with little temperature dependence. The temperature dependence was 0.055%/°C. The temperature variation can be improved to about 91% by the compensation technique. Therefore, our circuit can compensate for PVT variation of digital circuit performance drastically.

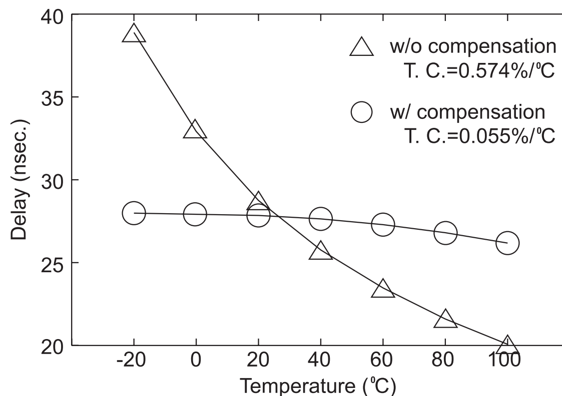

Fig. 10 Simulated propagation delay in critical path of 8-bit carry-look-ahead adder as a function of temperature in case with or without compensation circuit.

Table 2 Performance summary of our circuit.

Process	0.35 μm CMOS	
Temperature rang	−20°C – 100°C	
$V_{battery}$	2.6 V–3.6 V	
V_{DD}	1 V (TYP.)	
Power	141 μW (3.3 V)	
	w/ comp.	w/o comp.
Process sensitivity (σ/μ)	10.3%	36.1%
Temperature dependence	0.055%/°C	0.574%/°C
Line regulation	0.9%/V	—

Table 2 summarizes the characteristics of our circuit. The power dissipation of the circuit with a 3.3 V power supply was 141 μW at room temperature.

5. Conclusion

We developed a compensation circuit for low-voltage CMOS digital LSIs. At low-voltage operation, digital circuit performances vary significantly because of the threshold voltage variation. Our circuit can dynamically monitor and compensate for the variation of digital circuit performances. Its operation principle was confirmed with SPICE simulations. Process and temperature variations of digital circuits can be improved to about 71% and 91% respectively. Therefore, the proposed technique is useful for on-chip process, supply voltage, and temperature compensation of low-voltage digital circuits.

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